High Density RDL Technologies for Panel Level Packaging of Embedded Dies

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ABSTRACT

The ongoing miniaturization and functional heterogeneity in electronics packaging are pushing the demand for advanced substrate technologies. Highly integrated, advanced multi-chip packaging solutions combine application, logic and computing dies with memory or components for power management in a single package. A solution to achieve low fabrication costs is the close embedding of thin dies in IC Substrates based on large formats (600 x 600 mm²), known from PCB fabrication. In a consortium of partners from industry and research advanced technologies for Panel Level Packaging (PLP) are developed.

This paper will show the development of 5µm L/S RDL routing density and chips with 50µm bump pitch. Here, the 6x6 mm² dies are symmetrically embedded into an organic laminate matrix. A PCB core (100µm thickness) with very low coefficient of thermal expansion (CTE) containing laser cut cavities is used, acting as a frame layer. Besides mechanical and handling stability, the usage of such a frame offers the advantage of pre-integrating additional features like local fiducials, through vias or power lines by conventional PCB processes. Within that frame, the dies are embedded by lamination of an organic build-up film with 25µm thickness equal to bump height. The chip contacts are then opened without the need of any micro via formation. Here a strong focus is set on RIE etching of the polymer material.

Highly accurate measurement of the real die position is essential for the following processing. The formation of the redistribution layer (RDL) is done in a semi-additive process (SAP) utilizing sputtering technique and direct imaging (LDI). To achieve the fine pitch demands, an adaptive imaging process is applied. Therefore, a newly developed LDI machine is used to write structures in a 7µm photoresist. This exposure also combines the measurement data of the real die position and the adaption of the exposure artwork, in order to achieve highest registration quality.

Key words: panel level packaging, adaptive imaging, direct imaging, 3D system in package, IC substrate

INTRODUCTION

The scaling from wafer-level to panel-level is expected to be the next evolution of fan-out (FO) packaging [1]. However, there is still a technical gap between wafer front-end technologies and the PCB infrastructure. One major technological challenge to close this gap is to lower the structure size of lines and spaces (L/S) significantly. While L/S is going smaller, panel size is going up to 600 x 600 mm². To address these upcoming challenges of panel-level packaging (PLP) a consortium of German partners from industry and research develops advanced technology building blocks for PLP. The project aims for an integrated process flow with multi-die embedding in core using thin dielectric materials.

The feasibility of bare die embedding using FOPLP technologies has been demonstrated in recent publications [2], [3]. However, with downscaling to finer contact pitches on chips, below 60 µm and the potential misalignment challenge, gets even more difficult to overcome. In order to stick with reasonable production yield and time to market we are pursuing an adaptive process flow approach. Instead of costly accuracy improvements throughout the process chain the actual die positions are measured and the RDL wiring is adapted appropriately.

In the project consortium of German partners from industry and research, a new approach for PLP is investigated. The project aims for an alternative process flow for 3D SIPs with chips embedded into an organic laminate matrix, manufactured on large panels up to 600x600 mm² size [4]. The development will address the need for advanced packages, that combine application and memory dies with supportive components for power management in a single thin (< 200µm) and reliable package.

In the following sections the process concept and the current status of single process step development will be described.

PANEL LEVEL PACKAGING PROCESS

Concept and Technology

The basic PLP embedding concept is the use of a laminate core, in order to provide a high handling stability and also to achieve a limitation of the possible die shift during embedding. Therefore the core provides cavities at the position of the embedded dies, which are manufactured with only a little oversize compared to the die size. In addition the core can provide registration marks for global and local alignment for die placment and RDL formation, as well as premanufactured through vias and routing. The used core material is an organic glass reinforced PCB material, which will be structured with strandard print and etch technologies. To minimitze the CTE mismatch between core and embedded die, a low CTE material is used. The cavities at the die positions are cut by laser, and are designed to leave a surrounding gap of 40 µm larger than chip x-y dimensions is left. Figure 1 illustrates the concept.

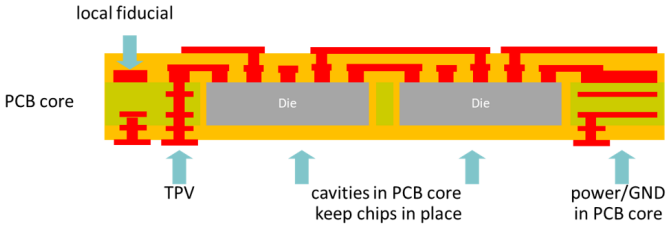

Figure 1: Schematic of PLP embedding concept

The technology utilizes processes known from the wafer backend, like sputtering of metal layer (PVD), plasma etching (RIE) of polymer material or semi additive Cu plating (SAP), and adapts these to the substrate world.

Another essential part is the use of dielectric materials. Here a strong focus is set on build-up materials, like Ajinomoto Build-up film (ABF), which is a non-photo sensitive film, or photo sensitive Polyimide like films, adapted from wafer backend.

The formation of the redistribution layer (RDL) is focused on semi-additive processing (SAP), which utilizes the deposition of barrier and seeding layers by PVD (Figure 2), high resolution photo-mask formation Figure 3), electrolytic copper plating and a final stripping of the photo resist and differential etching of seed and barrier. The detailed process flow will be explained in the following.

The concept provides a symmetrical embedding of bare dies into a core with cavities. The way of embedding generates low residual stress on the dies during embedding and soldering and the fabricated substrates exhibited very low warpage.

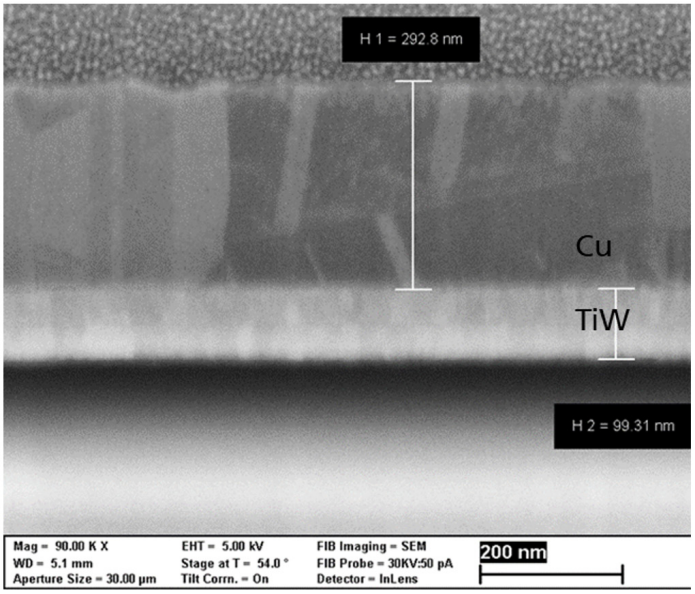

Figure 2: FIB cross section of sputtered Cu/TiW seed

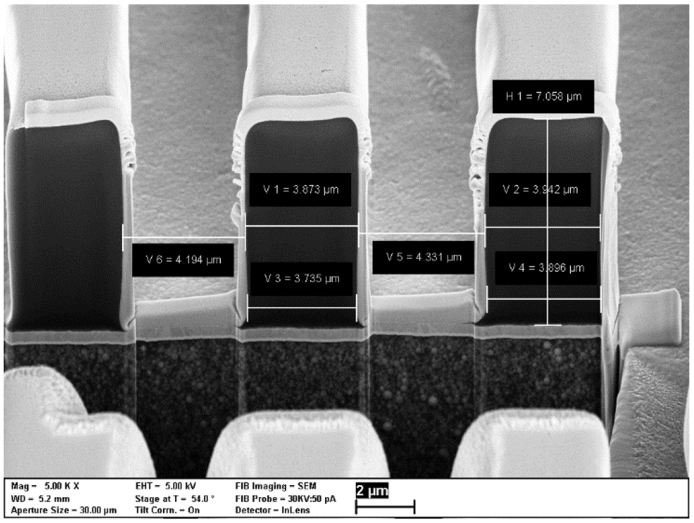

Figure 3: DFR with a thickness of 7µm exposed with a high resolution DI system: FIB section of a 4µm resist line

Demonstrator

The test vehicle is a 150µm thin module with two 6 x 6mm² dies. Both dies compromise 576 pcs. of 25µm high Cu pillars with a diameter of 60µm.At die surface daisy chain structures between the Cu connections allow electrical measurements. The demonstrator package has a size of 21mmx18mm. Core and dies have 100µm thickness. Three outer rows with a pad pitch of 50µm and 25µm pad diameter with pairwise on-chip outer interconnects for daisy-chain structures are placed at the outer chip area. The total I/O count is 1200. In the inner chip area, single bumps are arranged in cross-shape to support recognition in assembly machines. The fan-out is designed with 5 µm lines and spaces and pad openings of 15 µm diameter for contacting Cu pillars. This requires a via-to-pad tolerance of less than +/- 5µm.

In order to lower material cost, test panels were designed with a smaller size of 303x227mm² with 120 dual chip packages Figure 4.

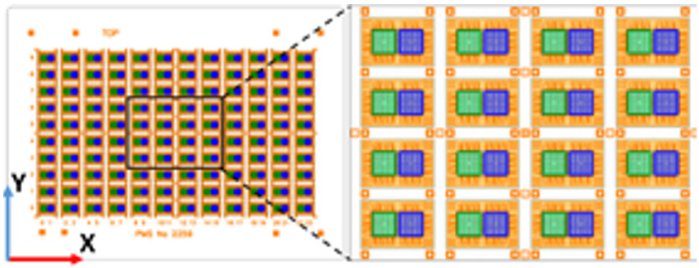

Figure 4: Substrate layout

In Figure 5 the schematic of the demonstrator package is illustrated.

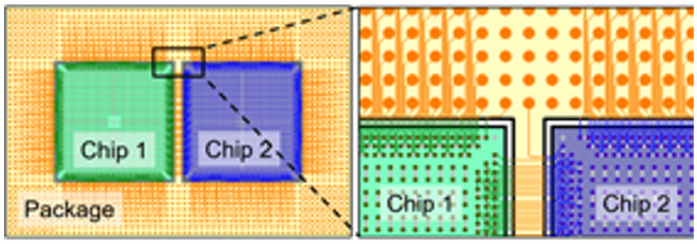

Figure 5: Demonstrator package layout

Adaptive processing

A flexible mask-less lithography system, a routing system and a packaging method were demonstrated in the late 1980s to handle the die position errors [4]. Also, compression molded multi die packages, fabricated as reconfigured wafers and panels from Deca Technologies Inc. use adaptive processes to solve die-shift issue during encapsulation [6].

In the following section, we present an embedding test vehicle with two bare dies in an organic substrate to demonstrate adaptive processes.

The basic principle of the adaptive approach is the use of actual data for each unique package on a substrate. Along the PCB process chain, each manufacturing step, like e.g. laser-direct-imaging, laser-drilling can fabricate the routing of even misaligned dies due to a layout correction. For this purpose, previously measured coordinates of the embedded components in relation to substrate coordinate system are utilized.

To measure the coordinates and rotation of the embedded dies a Coordinate Measurement Machine (CMM) capable, panel inspection tool (Rudolph Firefly S1200) is used.

Data of the die target coordinates and measured x- and y-shift and the rotation will be saved in a machine-readable ASCII format.

The yield of single die packages can be optimized by using methods of translation and rotation of the digital artwork. To connect two or multiple embedded dies with each other, it is not sufficient to move, rotate and scale the artwork only, because the angle and the direction of the die repositioning typically exceeds the pad tolerances.

To solve this task, the following method was evaluated, illustrated in Figure 6:

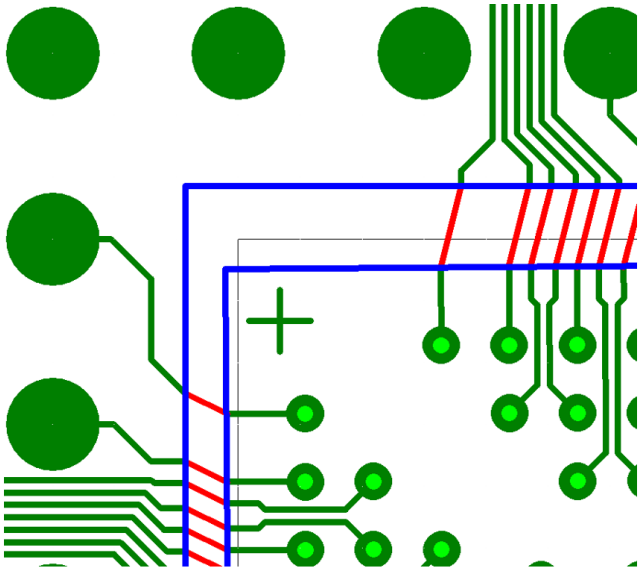

Figure 6: Rubber band method CAM Re-routing

Cutting areas (blue) around the die are defined, which allow artwork manipulation. An in-house developed software tool was used to calculate flexible, rubber band like connection traces (red), and relocatable plus fixed elements (green). The vertical die interconnects which are moving with the die pads are highlighted light green. In the shown example, the die was rotated 0.15°, and shifted -25 µm in x- and y-direction.

To manipulate the artwork, the CMM- and Gerber data of all CAM layers will be imported and all elements recalculated using a multithread optimized program code. Complete substrate fabrication data will be exported as Gerber-type for lithography and Excellon for laser drilling.

The successful use of adaptive imaging is shown in Figure 7. It demonstrates that the use of rubber band like RDL lines yields in well aligned interconnects and routing to the embedded die.

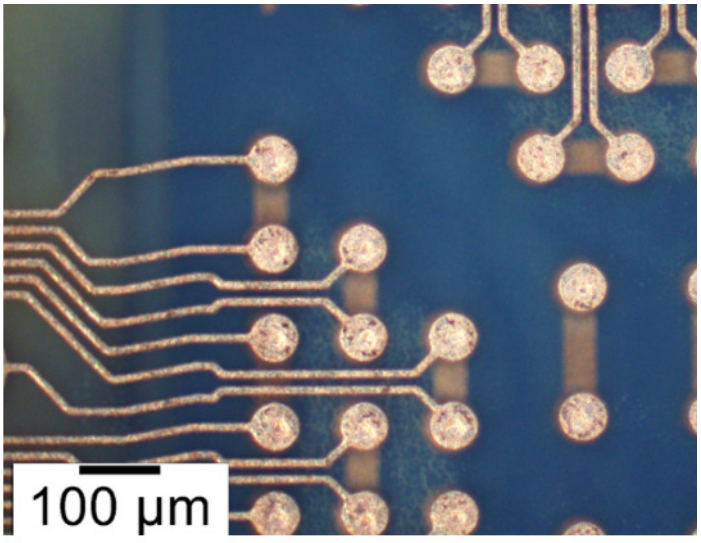

Figure 7: RDL layer with adapted layout

Package Realization and Results

As described, the demonstrator is a two die, one RDL layer configuration, like schematically shown in Figure 8

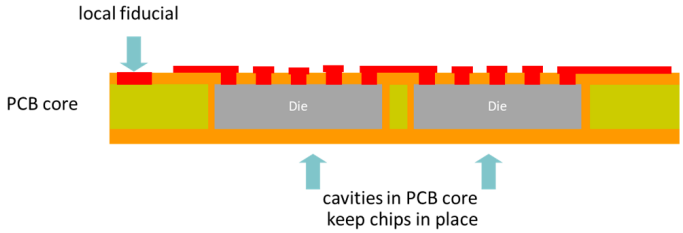

Figure 8: Schematic cross section of two die demonstrator

The overall process flow is shown in Figure 9 and will be described in detail in the following.

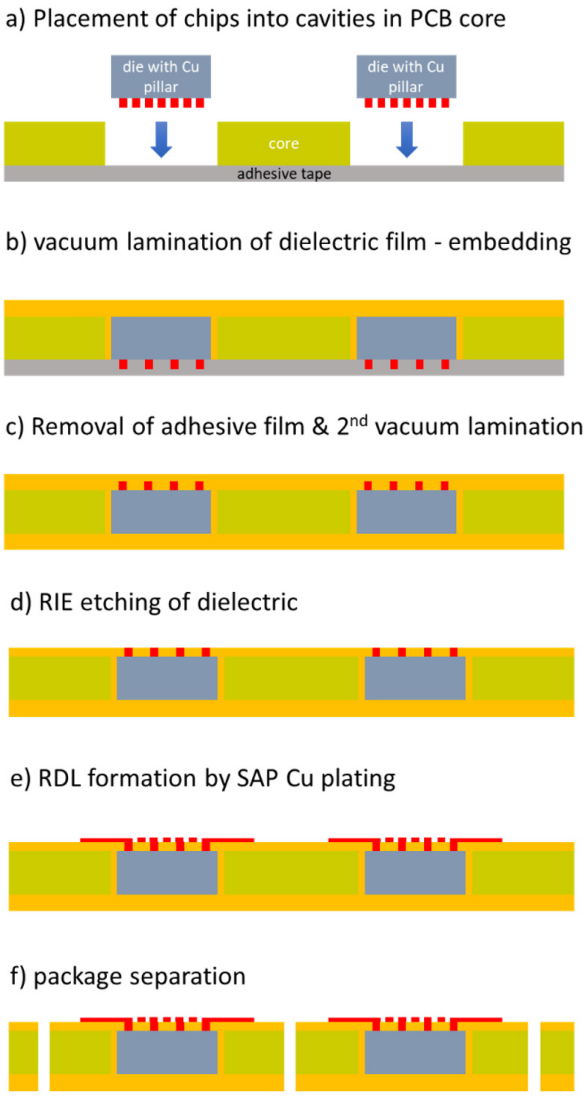

Figure 9: PLP process flow

Die placement

The die placement starts with the preparation of the core. After core structuring and cavity cutting, a single-side adhesive tape is laminated to the core substrate. Accordingly cavities are now equipped with a sticky bottom. A UV-releasable tape which has a 50 µm adhesive layer to allow full penetration of Cu bumps in the face-down assembly process is used.

Chip placement was performed with a die bond machine on 303 mm x 227 mm panel size and an assembly machine for larger panels. Since an adaptive approach is followed, the assembly accuracy is not the most crucial criterion.

Embedding

First step in embedding is the lamination of an Ajinomoto build-up film with (ABF) 25 µm thickness onto the backside of the core with the assembled dies, using a vacuum laminator. The gap between chip and core is filled during this process and results in a uniform backside. Next, a prebake step of 120°C for 30min until epoxy gelation takes place was applied. The pre-heating inhibits remelting of ABF in subsequent steps. The dies are now fixed in the cavities and the adhesive tape can be released by UV exposure. In order to remove possible remains of the adhesive layer, the substrates are treated with an oxygen plasma for cleaning. Now the dielectric film is laminated in the same way on the front side of the die, with the target to penetrate as deep as possible into the dielectric layer. The dies are now fixed and embedded in core cavities (Figure 10.)

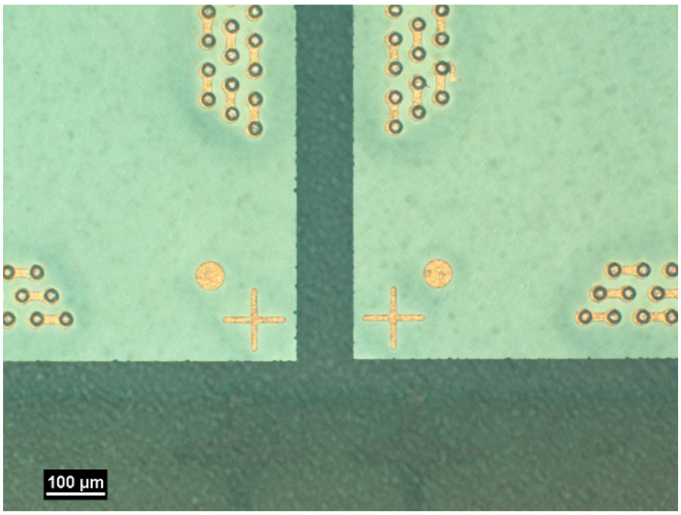

Figure 10: Die embedded in core cavity by ABF lamination

In Figure 11 an example of a substrate after dielectric film lamination is shown. It also illustrates the excellent handling ability of these substrates

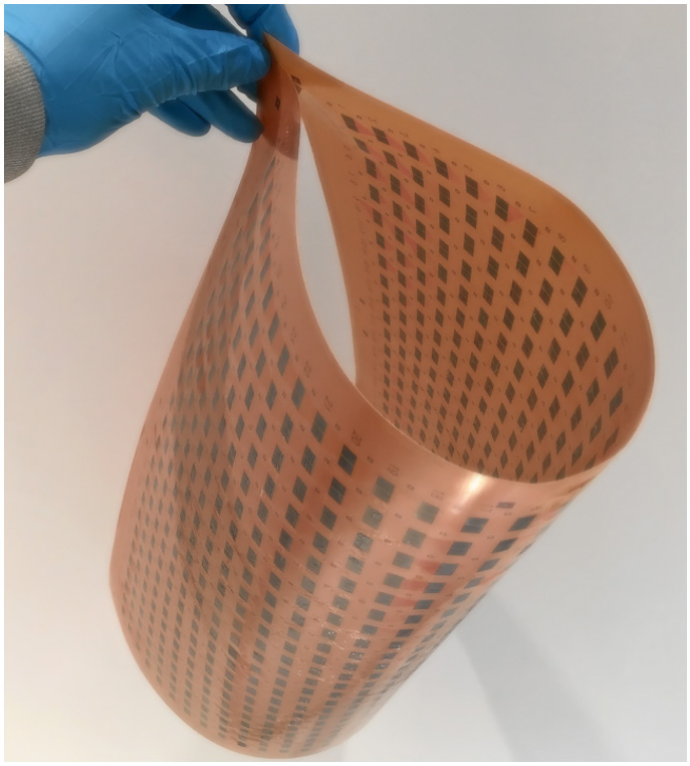

Figure 11: Substrate with embedded dies after dielectric film lamination

Adaptive RDL processing

After embedding, the die positions will be measured like described. The optical transparent ABF layer allows recognition of core fiducials and chip bumps. Hence, a file with real displacement vectors (x, y and rotation angle) will be created.

The artwork manipulation for the RDL layer of the two dies will be done like described.

Formation of Via to Chip

The next step is to reveal the Cu bump surface for subsequent electrical contact. Instead of the utilization of laser drilled vias, a different approach is used here. A reactive ion etching (RIE) process is considered for this task.

The first experiments were based on etching the dielectric by plasma completely on the full panel in order to reveal the Cu bumps. Here it was observed, that the homogeneity of plasma etching of only a few microns in z-direction over the complete panel area of several 100 millimeters is challenging to control. That's why the process was changed to the use of a metal hard mask, with openings at the contact positions only. The plasma etch process can then be designed to selectively remove the dielectric.

First, a Ti/Cu (100nm / 300nm) layer is sputtered onto the substrate front side. Then a 7 µm thin dry film photo resist is applied. For exposure a Laser Direct Imaging (LDI) machine is used. Since the bump positions are known from the coordinate measurement, an adapted image is applied, for opening the resist only at the appropriate locations (Figure 12).

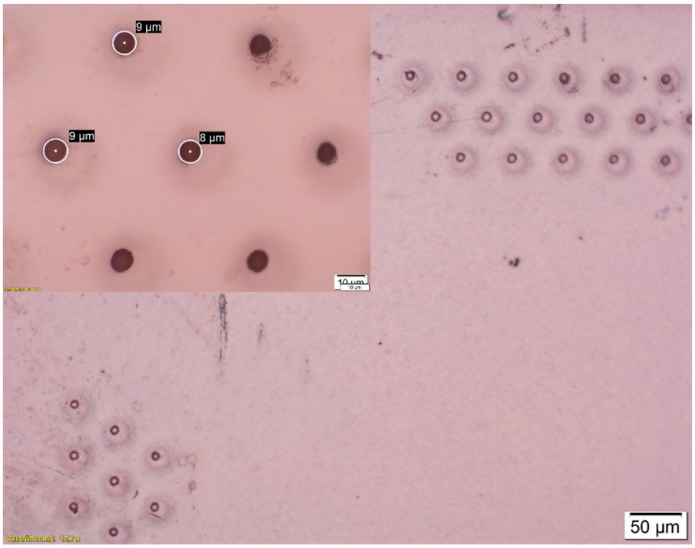

Figure 12: Openings in photo resist for structuring Ti/Cu hard mask for subsequent plasma etching

Afterwards, by chemical etching of Cu and subsequent resist stripping, a Cu mask for the Ti layer is defined. Now the Ti layer is etched, revealing the ABF surface only over Cu bump positions. The opening diameter of nominal 10µm is smaller than the bump diameter of 25 µm. The ABF is then etched utilizing RIE system.

Figure 13 show the scanning electron microscope (SEM) image of a focused ion beam (FIB) cut of such a plasma via.

About 5 µm of the dielectric have been selectively etched. The ABF surface surrounding the opening appears unaffected since it was covered by the metallic mask. No residues on the Cu bump are observed. There is an undercutting effect at the edge of the Cu bump. Concerning the reliability this is not an acceptable result. Further experiments will be carried out to optimize this process.

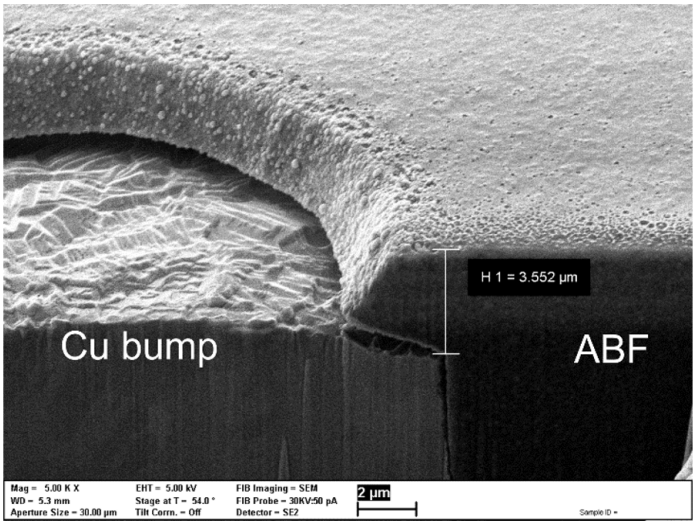

Figure 13: SEM of FIB cross section of a Plasma etched via opening

RDL formation

The formation of the RDL is done in the described semi additive process (SAP). After the sputtering of a 100nm Ti barrier and 300nm Cu seed layer a high resolution dry film photoresist is applied and structured by direct imaging (DI) exposure.

For the high resolution exposure, a digital micro mirror device (DMD) based direct imaging system is used. It is equipped with photo heads carrying a DMD with 2560 x 800 mirrors each. The light of a 405nm photo diode is reflected by switchable mirrors and guided through an optical system to project an image onto the photo resist. The optical system with a sub-pixel size of 360nm is designed for a lateral resolution of structures down to 4 µm. The photo heads move in strips over substrates with up to 620 mm x 620 mm size. The total exposure time for a panel depends on the number of photo heads (up to 6) and the required exposure dose of the resist.

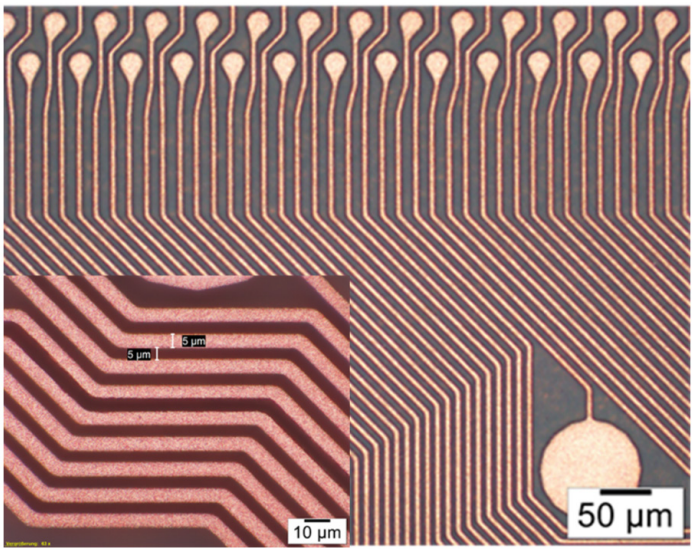

Figure 14: Cu RDL after SAP process

For the exposure of the high resolution DFR one photo head and an exposure dose of 550 mJ/cm² was used. With the given substrate size of 303 mm x 227 mm the resulting exposure time is about 10 min. Only four global fiducials per panel are required for registration, due to the adaptive process flow.

To minimize resist foot an oxygen descum plasma was applied after developing the exposed DFR. Following that, Cu plating is performed in a vertical automatic plating line. With a current density of 1.0 A/dm² Cu traces of about 6.5 µm thickness have been plated with a growth rate of about 0.25 µm/min. Then the resist is stripped. Finally, by differential etching the initial Cu seed and Ti barrier layer were removed. Figure 14 and Figure 15 show the demonstrator fan-out design with 5 µm line/space after SAP process.

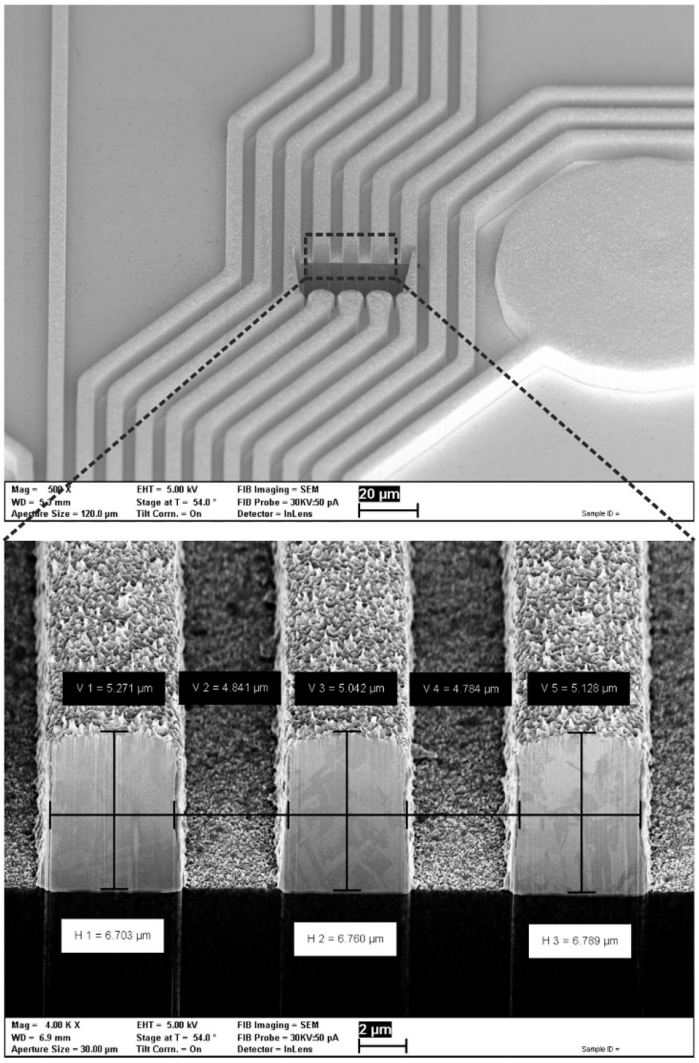

Figure 15: FIB section and SEM view of Cu RDL after SAP

SUMMARY

A new approach for panel-level packaging is currently developed. This approach focuses on the use of a PCB laminate based core material and thin dielectric films. In order to avoid laser drilled micro via connections to the embedded components, copper pillar structures and plasma etched vias are of interest for connecting the die to the RDL. The current development work is done on smaller panel sizes of 303x227cm².

The fan-out redistribution layer with 5 µm L/S Cu traces were grown in a semi-additive process with sputtered Ti/Cu seed layer on organic substrates. For direct imaging of the plating mask a digital micro mirror based direct imaging machine was used. With mask-less technology the build-up images can be recalculated and adjusted to individual, actual die position (adaptive imaging).

Next steps will include the optimization of process capability (fine line SAP, plasma etching) and scaling to panel sizes up to 610mm x 615 mm.

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