Miniaturized Stacked Die QFN for Tire Pressure Monitoring System Applications

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ABSTRACT

Tire Pressure Monitoring Systems (TPMS) are electronic wireless systems that monitor and report air pressure inside pneumatic tires in real time. An example of a TPMS module integrated with the valve stem and showing the typical tire mounting location is shown in Figure 1. For their safety and fuel economy benefits, starting with the mid-2000's, active TPMS were mandated on many vehicles worldwide. The National Highway Traffic Safety Administration (NHTSA) estimates that there are approximately 23,000 accidents and 535 fatalities annually involving tire underinflation and blowouts [1]. The use of TPMS has been shown to result in improved fuel economy and therefore reduced carbon emissions [2]. TPMS in passenger vehicles was mandated in the US as of Sept. 1, 2007 under the Transportation Recall Enhancement, Accountability and Documentation (TREAD) Act, in the European Union as of Nov. 1, 2012 and in South Korea as of Jan.1, 2013. Countries like Russia, Indonesia, the Philippines, Israel, Malaysia, Turkey and many others soon followed [3].

The first TPMS systems were large and bulky with a significant electronics content [4]. Since that time TPMS electronics have gotten more energy efficient and form factors have come down dramatically. This paper will outline an effort to miniaturize an existing 1.0 mm pitch, 7x7x2.2 mm body size 24 lead QFN (Quad Flat No Leads) TPMS down to a 4x4x1.98 mm body size QFN with 0.5 mm pitch that would still meet Automotive Electronics Council (AEC) Grade 1 reliability requirements. The original 7x7 mm three die QFN package consisted of an ASIC, a pressure sensor and an accelerometer. This miniaturization led to many technical challenges at both the package and board level. This paper will primarily address the board level reliability (BLR) challenges encountered due to the large silicon to package ratio along with the 50% reduction in pitch. Through a series of test vehicles with variables such as QFN leadframe surface finish, lead shape and size, wettable flank (WF) technology and anchors pads, the BLR was successfully improved to the point where it met application requirements.

Key words: QFN, Board Level Reliability (BLR), Tire Pressure Monitoring System (TPMS), pre-plated leadframe (PPF), intermetallic compound (IMC), step-cut, dimple.

INTRODUCTION

An integrated TPMS solution, pictured in Figure 2, was introduced in 2014 in a 7x7x2.2 mm 24 QFN with 1.0 mm lead pitch with nominal 0.60 mm wide package perimeter Input/Output (IO) pads. As can be seen in Figure 3, it had dimpled NiPdAu pads in the leadframe to enable wettable flanks and therefore inspectable solder joints which are typically required by automotive [5]. At only 0.3 grams, it was the smallest available when introduced in 2014 [6]. The 7x7 mm QFN included a micro-electromechanical system (MEMS) accelerometer die to detect wheel motion to save battery life, a MEMS pressure sensor with a range of 100–900 kPa (14.5 – 130.5 psi), an integrated temperature sensor, an integrated ASIC microcontroller, and RF transmitter and low frequency receiver capabilities.

Figure 1: TPMS module showing location within the wheel.

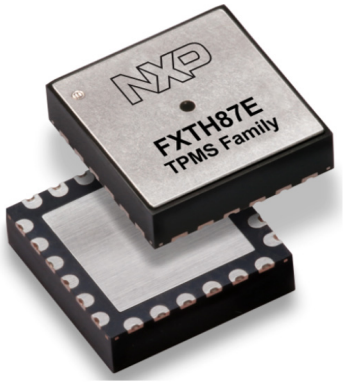

Figure 2: Existing high volume manufacturing (HVM) TPMS three die module in 7x7x2.2 mm, 0.5 mm pitch QFN.

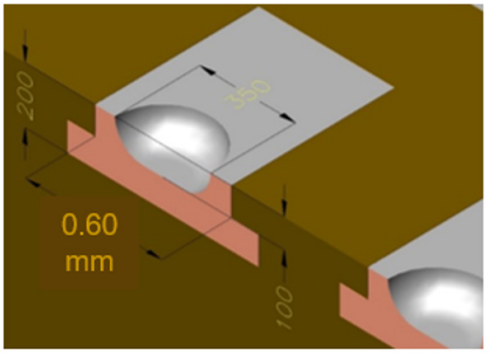

Figure 3: Dimpled NiPdAu plated IO pad on the 7x7 mm QFN to enable wettable flanks and inspectable joints.

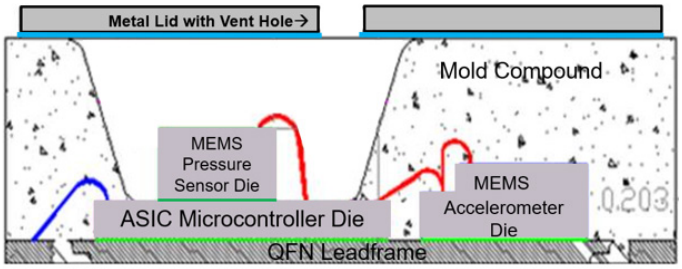

Figure 4: Side by side and stacked layout of the three die in existing HVM 7x7 mm QFN.

As can be seen in Figure 4, the prior 7x7mm TPMS module had all three die on the exposed pad die flag of the QFN with the MEMS pressure sensor die stacked on the Application Specific Integrated Circuit (ASIC) microcontroller die. Note that the dimpled IO leads are not depicted in this Figure. The QFN featured a metal lid with a vent hole to allow exposure of the MEMS pressure sensor to the pneumatic pressure within the tire.

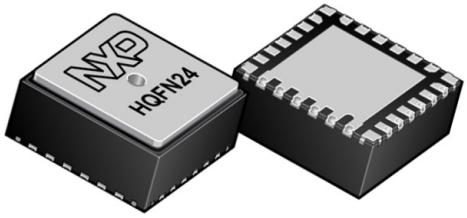

Figure 5: Miniaturized 4x4 mm QFN for TPMS.

To enable smaller form factor, more cost effective TPMS modules by customers, a project was undertaken to shrink the 7x7 mm to a 4x4 mm QFN. The primary challenge was to fit the same three die functionality into a package with a 67% smaller x-y form factor that resulted in very large microcontroller die to package area ratio of 57%. Equally challenging is meeting the board level reliability requirements at the shrunken 0.5 mm lead pitch. Although it will not be covered in this paper, another challenge of course was to meet overall AEC Q100 Grade 1 component-level reliability requirements [7]. Figure 5 shows the miniaturized 4x4x1.98 mm TPMS module. It appears visually very much like the 7x7 mm, but internally both MEMS die had to now be stacked onto the ASIC microcontroller. And, as can be seen in Figure 6, the ASIC die is actually larger than the new, smaller die flag such that it rests on the IO pads along one side of the package.

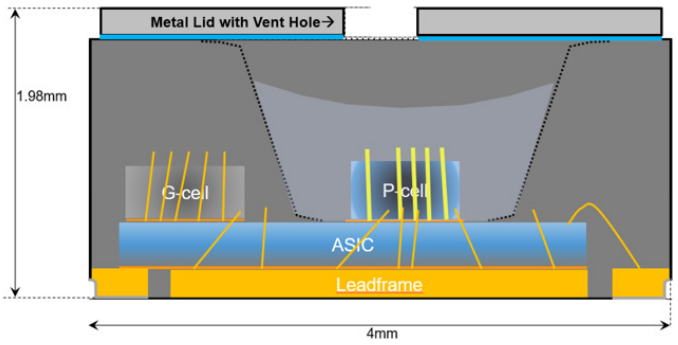

Figure 6: Internal configuration of the 4x4 mm TPMS QFN showing both MEMS die stacked onto the ASIC. Also, note the ASIC die is larger than the die flag on the leadframe such that it rests on IO pads on one side (left side above).

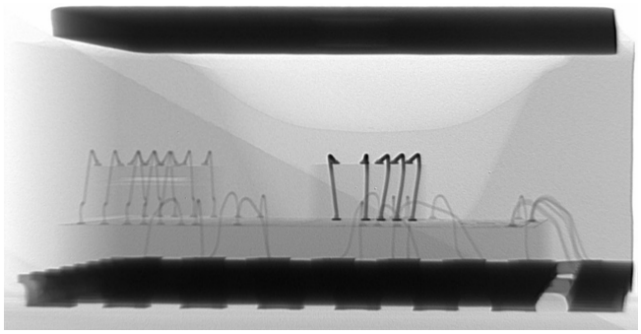

Figure 7: X-ray of the 4x4 mm TPMS QFN showing the die and wire bond configuration. The dark area at the top is the lid which has a vent hole that is not visible in the X-ray.

MINIATURIZED 4X4 MM QFN BOARD LEVEL RELIABILITY EVALUATIONS

Test Vehicle One Details

An initial miniaturized 4x4 mm QFN test vehicle (TV) was designed. It is pictured in Figure 8 and utilized Sn plated surface finish. Since it was Sn plated it employed the step cut process for the IO leads to achieve wettable flanks. A cross-section of a typical Sn plated lead with a step cut is shown in Figure 9. The leads were designed at 0.250 mm wide nominally and no anchor pads were used. Anchor pads are pads in the corner of the QFN that are typically not connected electrically but may be soldered to the PCB.

A daisy-chain was formed on the first test vehicle by wire-bonding adjacent IO pads. Double lead to lead wire-bonds were used to help ensure no wire bond failures were encountered in the testing. The pads on one side of the package where the ASIC die was resting on the pads due to its size were not included in the daisy-chain. These are also no connect pads on the product. A schematic of the package and PCB daisy-chain routing used for this test vehicle as well as subsequent ones is shown in Figure 10.

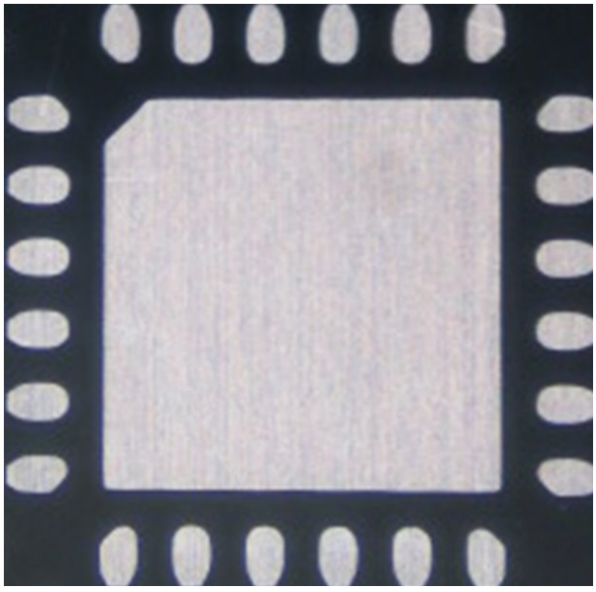

Figure 8: Bottomside image of the first 4x4 mm 24 QFN test vehicle used for board level reliability. Note the Sn plating.

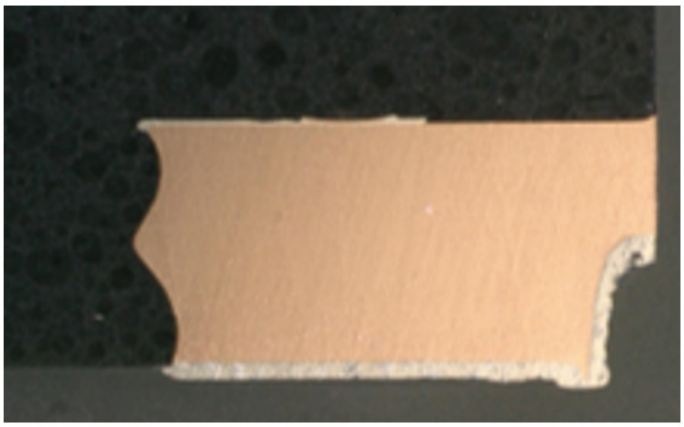

Figure 9: Cross-section of a lead on TPMS 4x4 mm 24 QFN 1st test vehicle showing the Sn plated step cut. This is an alternative way to achieve wettable flanks compared to the dimple shown in Figure 3.

The daisy-chain parts were assembled to PCBs using a SAC305, ROL0, type IV powder, no clean solder paste. The 1.57 mm thick high Tg FR-4 PCBs with OSP surface finish used for BLR testing used 0.275 x 0.85 mm pads for the QFN IOs. The 0.1 mm thick stencil openings were 1:1 with the IO pads and provided 63% areal coverage on the exposed pad. Figure 11 shows the PCB footprint with a typical solder paste print prior to component placement and Figure 12 shows a cross-section of a typical time zero solder joint. Reflow with a 240°C peak temperature in air was used. After assembly the PCBs were placed into single chamber, 15 minute ramp and dwell, one hour total, -40 to 125°C thermal cycle. Continuous, in-situ continuity monitoring with high speed event detectors was used during the cycling to detect failures.

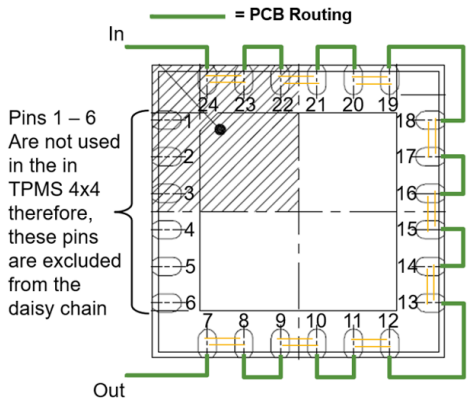

Figure 10: 4x4 mm QFN daisy-chain routing on both QFN and PCB. Die not shown here but were present on the TV's.

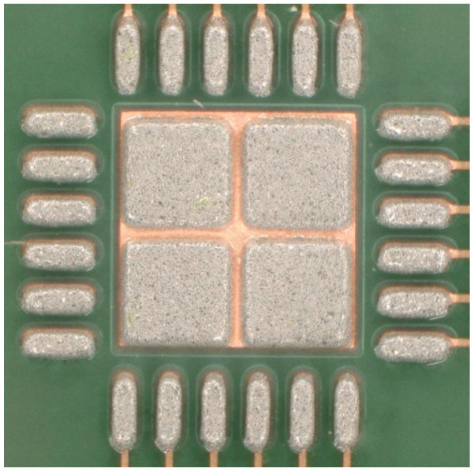

Figure 11: PCB design and solder paste print used for the 4x4 mm QFN test vehicle 1. IO pads were printed 1:1.

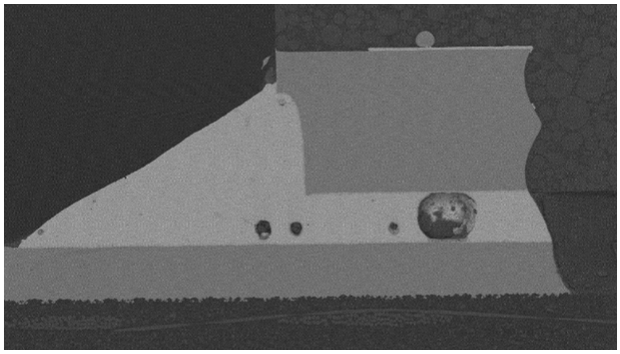

Figure 12: Typical solder joint cross-section on the 1st TV. Note the step cut in the lead resulting in a wettable flank.

Test Vehicle One BLR Results

BLR results obtained with 1st TV design were somewhat worse than expected with 1st fail at approx. 300 -40 to 125°C cycles. This can be seen in the Weibull plot of results in Figure 13. As can be seen in Figures 14 and 15, failure analysis showed interfacial failures between the intermetallic compound (IMC) on the lead and the bulk SAC305 solder.

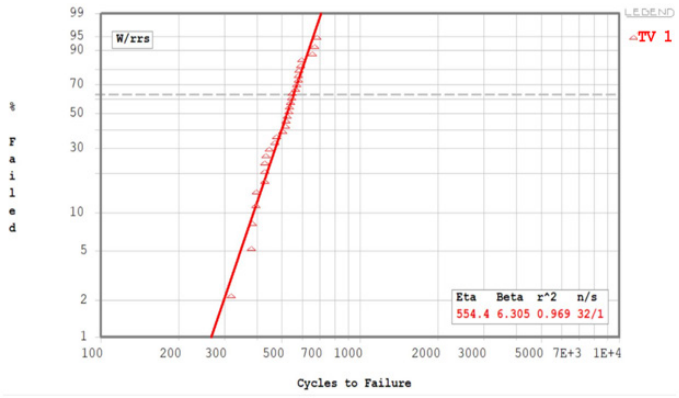

Figure 13: Weibull plot of BLR results for the first 4x4 mm QFN TPMS TV showing 1st failure at approx. 300 cycles.

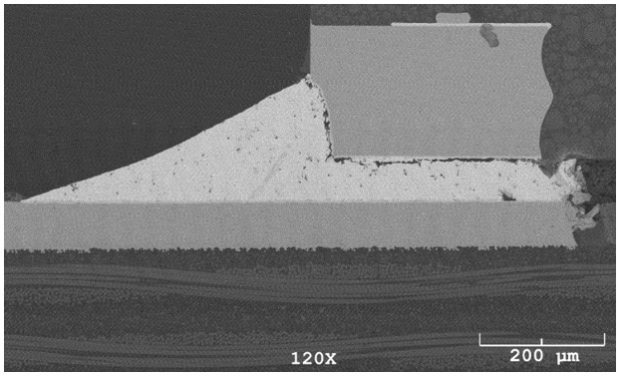

Figure 14: Cross-section of a BLR failure on the 4x4 mm QFN TPMS TV showing interfacial fracturing between the bulk solder and the QFN lead. See higher mag image below.

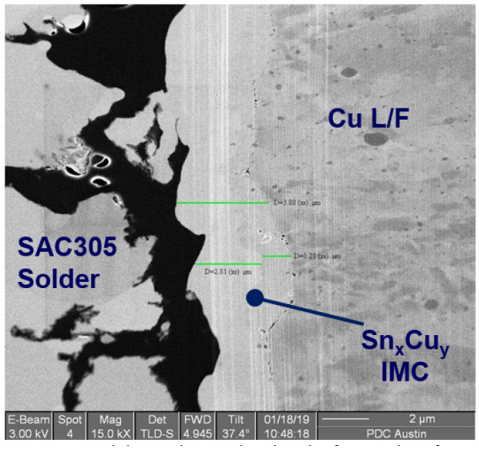

Figure 15: High mag image showing the fracture interface.

Test Vehicle Two Details

Given the less than desirable results obtained with the 1st TV, a 2nd TV was designed with some attempted improvements. These improvements included fusing unused pads 1-6 to the exposed pad, adding corner anchor pads with step-cut leads and IO pad sizes were increased to 0.275 mm width. A comparison of the 1st and 2nd TV's is given in Figure 16. Also, as can be seen in Figure 17, the PCB and accompanying stencil design were altered to match the 2nd TV's features.

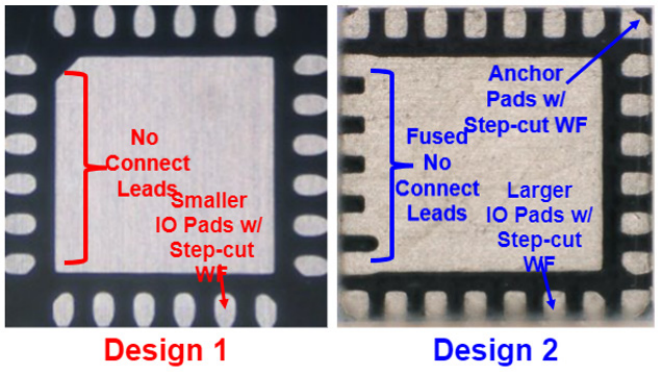

Figure 16: 4x4 mm QFN TV designs 1 and 2 comparison.

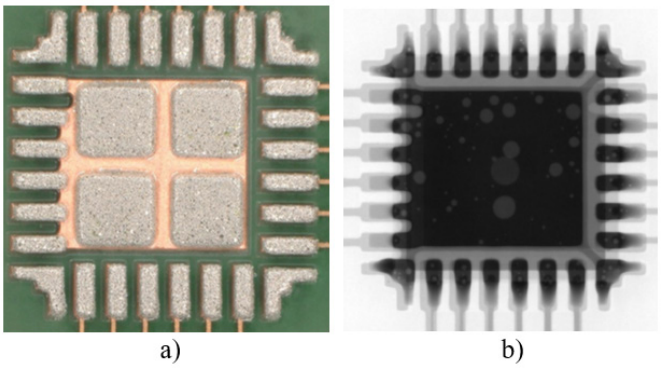

Figure 17: Images of the a) PCB design and solder paste print and b) post-SMT assembly X-ray for the 4x4 mm QFN test vehicle two. Note typical voiding on the exposed pad.

Test Vehicle Two BLR Results

As can be seen in Figure 18, BLR results obtained with a 2nd TV were only marginally better than the 1st design with 1st solder joint failure at approximately 430 cycles. Failure analysis showed a similar failure mode of IMC to solder interfacial fracturing as the 1st TV.

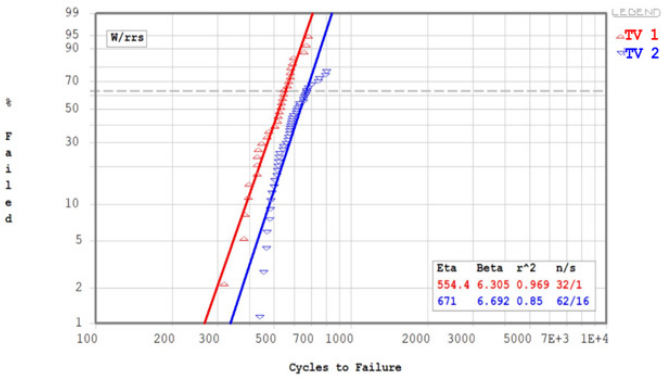

Figure 18: Weibull plot of BLR results for the 1st and 2nd 4x4 mm QFN TPMS TV's showing little improvement.

Test Vehicle Three Details

As can be seen in Figure 19, a 3rd 4x4 mm QFN TV was then designed, but this time using a NiPdAu surface finish. Dimples where incorporated to achieve wettable flanks as opposed to the step-cut Sn plated leads on the 1st and 2nd TV's. Refer back to Figure 3 for an example of a dimple. QFN pads were also designed to have less taper at the package edge thereby further increasing the lead area for soldering. The six pads that were fused to the exposed pad from the 2nd TV were retained.

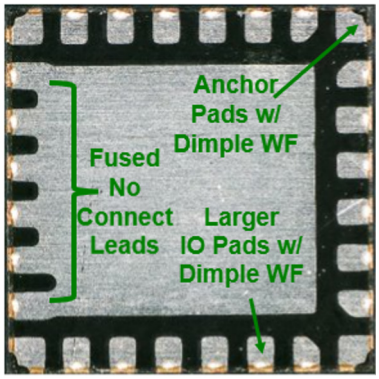

Figure 19: 4x4 mm QFN 3rd TV design which is NiPdAu.

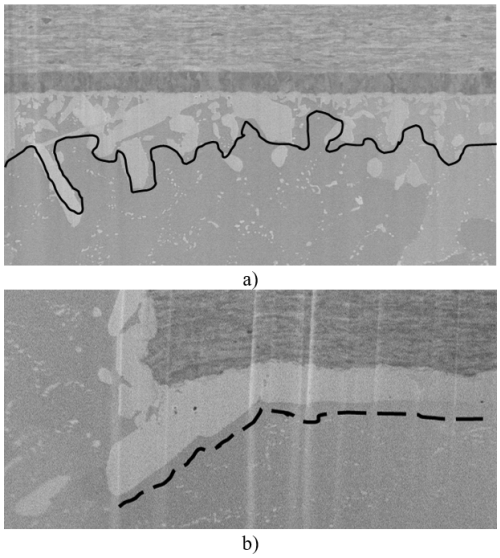

Figure 20: Comparison of the IMC formation observed on the a) NiPdAu versus b) the Sn plated surface finish QFN following PCB mount. Note the rougher IMC on the NiPdAu sample leading to greater interlocking with the bulk solder.

Time zero cross-sections of the 3rd TV parts following mounting to PCBs showed a different IMC formation for the NiPdAu surface finish than was previously observed with plated Sn. As can be seen in Figure 20a, the rougher IMC formation on the NiPdAu leadframe led to a higher degree of IMC to solder interlocking. Figure 20b shows the IMC formation on a Sn plated part from the 1st TV for comparison.

Test Vehicle Three BLR Results

BLR results obtained with the 3rd and final TV were dramatically better than the 1st and 2nd designs with 1st fail at greater than 1500 -40 to 125°C cycles. The results for all three TV's are plotted in Figure 21. Failure analysis following BLR on the 3rd TV showed a much different failure mode versus the previous Sn plated TVs. As can be seen in Figure 22, the solder joint fracturing was predominantly through the bulk SAC305 solder with this 3rd TV.

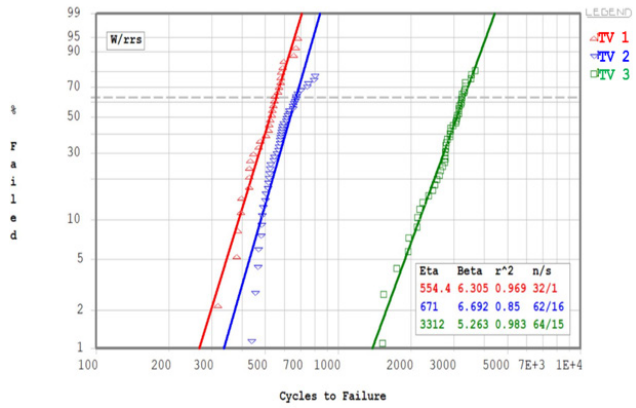

Figure 21: Weibull plot of BLR results for the 1st, 2nd and 3rd 4x4 mm QFN TPMS TV showing vast improvement for the 3rd TV.

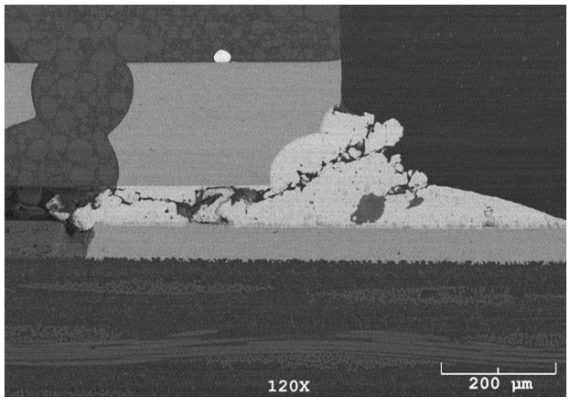

Figure 22: Cross-section of a failure following BLR testing of the 3rd 4x4 mm QFN TV with NiPdAu surface finish. Note that the fracturing is predominantly through the bulk solder as compared to TV's one and two where the fracturing was at the interface between the IMC and the solder.

SOLDER NANOINDENTATION RESULTS

In order to better understand the performance difference between the two surface finishes, extensive bulk solder nanoindentation was carried out on time zero NiPdAu versus Sn plated leadframe QFN samples mounted to PCBs [8]. As can be seen in Figure 23, significantly higher solder hardness was observed near the IMC to solder interface for the NiPdAu leadframe sample. Looking at the hardness values right at the package IMC interface (Row 6 in Figure 23a and 23b), the values are over 50% higher on the NiPdAu sample (<0.30 versus 0.45 GPa).

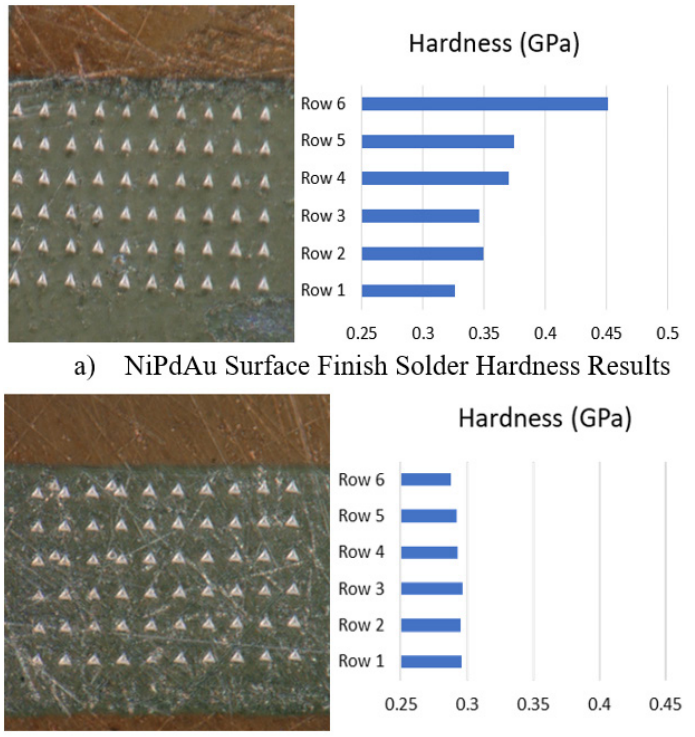

Figure 23: SAC305 solder nanoindentation results on a) NiPdAu versus b) Sn plated surface finish QFN's. Significantly higher solder hardness was observed near the IMC to solder interface for the NiPdAu leadframe sample.

CONCLUSIONS

The existing 7x7 mm TPMS QFN was successfully miniaturized to a 4x4 mm QFN that meets BLR expectations for the intended application. The stresses resulting from the high die to package area ratio were overcome by:

- Maximizing the size of the QFN IO pads, including the width at the package edge.
- Fusing unused leads on one side to the exposed pad to increase the overall copper content of the package.
- The use of non-electrically connected anchor pads in the four corners which also incorporated wettable flanks.
- Most importantly, the use of a NiPdAu surface finish which also incorporated dimpled leads for wettable flanks.
- NiPdAu surface finish was found in general to be more resistant to the high interfacial stresses generated between the package and solder encountered on this package. This was found to be due to the more complex and rougher IMC formed by the NiPdAu finish which led to more solder to IMC interlocking as well as increased hardness of the solder near the IMC.
- It should be noted that the NiPdAu improvement affect is believed to be less for cases with lower overall solder to pad interfacial stresses.

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BIOGRAPHIES

Andrew Mawer is the Global Package Design Manager at NXP Semiconductors in Austin, TX. Immediately prior to that he managed an analytical and reliability laboratory. Andrew has been with NXP, formerly Motorola then Freescale for a total of 28 years. Andrew previously spent four years at HP where he was involved with the implementation of some of the first high pin count PBGAs in the industry. He has authored and presented over 40 papers and authored two book chapters. He is an active member of SMTA and has served on the Technical Committee of the SMTA-I Conference, the Review Board of the SMTA Journal

and with various leadership roles within the Central Texas SMTA chapter. He received the SMTA National Member of Technical Distinction Award in 2007. Andrew received his B.S. in Mechanical Engineering from the University of Texas in 1987 and M.S. in Mechanical Engineering from Rice University in 1989. He received the Outstanding Young Mechanical Engineer Award from UT's Mechanical Engineering Dept in 2007.

Mollie Benson works at NXP Semiconductors in Austin, TX as a Packaging Engineer for Analog and Mixed Signal Packaging. She previously supported the Product Diagnostic Lab for three years, where she managed the Board Level Reliability and Package Analysis activities. Mollie joined NXP in 2017 and has had a variety of packaging experience including Board Level Reliability (Thermal Cycling and Shock, Monotonic Bend, and JEDEC Drop testing), SMT assembly, PCB design, and failure analysis. Mollie has a Bachelor of Science degree in Materials Engineering from California Polytechnic State University, San Luis Obispo.

Dwight has been in Semiconductor Product Engineering and Packaging since 1984. He started his career at Motorola Semiconductor Product Sector supporting logic devices in relatively small, simple packages. Since then he has moved to a development lab where he spent several years working on IC's in high reliability packages for government projects, followed by packaging of Gate Arrays in high pin count QFP, BGA and thermally enhanced packages. He's developed packages and processes for digital image sensor assembly and RF handset modules. Most recently Dwight has been working on the challenges of packaging motion and pressure sensor devices for consumer and automotive applications. Dwight holds 20 US patents, has been published in multiple trade journals, proceedings and magazines and has served on the editorial review board of 1 industry magazine.

A R Nazmus Sakib performed this work at NXP Semiconductors in Austin, TX as an IC Packaging Materials Engineer during his tenure from May 2017 to March 2021. He is currently employed as Staff IC Packaging Engineer at Renesas Electronics America in Austin, TX. During his time at NXP, he was involved in die attach, underfill and solder material characterization, material selection and deployment for various packaging technologies such as QFN, FCPBGA, Wire bonded BGA etc. Sakib has hands-on experience with DMA, TMA, DSC, TGA and Nanoindentation. Sakib has a Bachelor of Science degree in Mechanical Engineering from Bangladesh University of Engineering and Technology and a PhD in Mechanical Engineering from University of Texas at Arlington.

Vishrudh Sriramprasad is starting a Masters in Sustainable Engineering at Arizona State University in the Fall of 2021. In May of 2021, he graduated with a Bachelor of Science in Mechanical Engineering from the University of Texas at Austin. During the summer of 2020, Vishrudh interned at NXP Semiconductors as a Reliability and Package Analysis Intern. At NXP he learned how to pot, image, and analyze failed package samples in an SEM. He specifically worked with the TPMS 4x4 and PF7100 packages during his internship. Looking forward, Vishrudh hopes to contribute towards research in the field of direct air carbon capture at ASU and promote sustainable energy practices and policies.