INVESTIGATION OF SOLDER JOINT ENCAPSULANT MATERIALS FOR DEFECT MITIGATION

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ABSTRACT

As next-generation networking equipment continue to push the trends of higher signal speeds and increased functional density, the need for advanced PCB structures, such as Via-in-Pad Plated Over (VIPPO) and backdrill, and high-speed memory is becoming more mainstream across product platforms. Furthermore, as these high-speed memory technologies are being driven by consumer applications, the form factor and interconnect pitches continue to shrink to meet the demands of the mobile device market. The use of these advanced PCB structures, like VIPPO and VIPPO with backdrill, within the BGA footprints, particularly for the fine pitch patterns, have been found to result in BGA solder separation defects at the bulk solder to IMC interface upon a 2nd reflow, e.g. during top-side reflow for bottom-side components or during rework of an adjacent BGA.1 This type of solder separation occurs during reflow and is associated with out-of-plane CTE mismatch underneath adjacent BGA pads as well as a differential in the time to reach liquidus for adjacent BGA solder joints due to disparities in thermal conductivity of those areas underneath the adjacent BGAs. It is not a non-wet or solder fracture in that there is a properly formed intermetallic compound (IMC) layer between the Cu pad and the solder and the separation occurs between the bulk solder and the IMC and is not initiated at a crack. In some cases, this solder separation failure mode has also been identified with buried vias under the BGA pad. 2.3 Additionally, small memory components have been experiencing high occurrences of head-in-pillow (HIP) defects even though the overall package warpage over the reflow profile is < ~3mils.

This paper will therefore focus on the mitigation of these solder joint defects resulting from SMT assembly with the use of solder joint encapsulant materials to provide enhanced adhesion strength for the solder joints. Leveraging existing test vehicles that are known to induce the aforementioned solder joint defects, two different solder joint encapsulant or epoxy flux materials are evaluated in terms of the application process, assembly integrity and compatibility with standard SAC305 production solder paste materials and SMT processes.

Key words: BGA solder joint defects, Head-in-Pillow (HIP), BGA solder separation, epoxy flux, solder joint encapsulant, SMT assembly, Via-in-pad plated over (VIPPO), solder hot tear, solder joint reliability, ATC testing

INTRODUCTION

With the trend of increasing signal speeds, board functional density and PCB layer count/thickness, PCB structures and designs are becoming more complex, and are resulting in new or unique solder joint defects during assembly. As discussed previously, increased occurrences of the solder separation defect have resulted with the introduction of the mixed VIPPO BGA footprint designs within the PCB. Moreover, the occurrence of HIP defects on small body BGA packages with very low package warpage over the reflow profile has emerged as well. Typically, these HIP defects are attributed to PBGA packages with high package warpage characteristics over the reflow profile. These types of HIP defects can be addressed by either modifying the package design and/or modifying the SMT reflow process. In order to optimize the package design for improved warpage behavior, the package design can be rigidized or modified to minimize the effects of the CTE mismatch within the package. For instance, using a stiffener ring with heat spreader instead of a top-hat lid design and employing a thick core (e.g. 800um or 1.2mm core thickness) substrate will increase the stiffness of the package and help to control the magnitude of the package warpage experienced over the reflow profile. Additionally, optimizing the underfill material properties to reduce the chip-to-package interaction (e.g. having a lower Tg) can also help to minimize the resulting package warpage. In terms of the SMT process, the reflow profile and process can also be optimized to mitigate HIP defects by reducing solder oxidation, minimizing flux exhaustion prior to reflow and allowing for more time during reflow for the solder ball and paste to coalesce. This can be achieved with the use of nitrogen to create an inert environment during SMT, reducing the soak time and increasing the time above liquidus. Finally, these HIP defects can also be mitigated by controlling the printed solder volume on the BGA pads as a function of the location and the package warpage in that area. However, for these new HIP defects that are not dependent on the package warpage, these SMT process parameters may not be sufficient to mitigate the defects and alternative mitigation strategies become necessary.

The primary objective for this evaluation is, therefore, to assess the effectiveness of two different solder joint encapsulant or epoxy flux materials in terms of their ability to mitigate both the solder separation defects associated with the use of VIPPO within the PCB BGA footprint as well as the HIP defects for small BGAs with < 3 mils warpage. These encapsulant materials being investigated in this study provide an attractive alternative to underfill materials as they can be assembled in-line without the need for additional specialized equipment. Furthermore, these materials can be cured during reflow, and hence, do not require additional processing steps and do not significantly increase cycle times.

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Existing test vehicles that have exhibited both of these defects will be employed for this study. These test vehicles will be assembled with each of the solder joint encapsulant or epoxy flux materials included within this study. Ease and performance of the application process for each of the materials will be evaluated. Additionally, inspection and physical analysis will be used to assess the solder joint integrity to understand the effectiveness of these materials for defect mitigation. Finally, these materials will also be evaluated in terms of their compatibility with existing production materials and processes.

EVALUATION PLAN

Two existing test vehicle designs have been implemented for this investigation. These test vehicles have previously been demonstrated to induce both the solder separation defect with a mixed VIPPO/non-VIPPO BGA footprint as well as the HIP defect for small BGA packages with very small package warpage over the reflow temperature excursion. In addition, two different solder joint encapsulant materials are targeted for this study, both of which employ a similar application process that can be incorporated in-line with conventional SMT equipment. Both encapsulant material manufacturers cited their materials to be compatible with standard SAC305 solder paste systems.

A dip process was implemented within the pick and place equipment (after the solder printing process) in order to apply the encapsulant materials to the BGA balls of each component, similar to a flux dip process. For this process, the pick and place equipment uses a dip tray filled with the encapsulant material. As illustrated in Figure 1, during pick and place, the component was picked up, dipped into the encapsulant material and then placed onto the printed solder of the PCB pads. The amount of encapsulant material applied to the BGAs was controlled by the depth of the dip tray. For these evaluations, a dip depth of 85% of the BGA diameter was used to ensure adequate coverage of the encapsulant up to the BGA package pad interface. Dip dwell times ranged from 0.3 to 1 sec, depending on the encapsulant material and BGA diameter/pitch. These encapsulant materials were then cured during the SMT reflow process. Therefore, there are no additional handling or process steps required for implementation of these encapsulant materials. Both of these materials are also advertised to be reworkable with standard BGA rework processes, but that is beyond the scope of this investigation.

For this investigation, each of the test vehicles includes a set of control boards, a set of boards with parts dipped in encapsulant A and a set of boards with parts dipped in encapsulant B. Each of these boards is evaluated after SMT assembly via x-ray inspection techniques with 1 board of each set also subject to physical analysis. The remaining boards are then subject to a 2nd reflow in order to simulate a secondary top-side reflow process. This was conducted to attempt to induce the solder separation defect. Again, each of the boards was inspected via x-ray with 1 board of each group subject to physical analysis. Finally, the remaining boards were submitted to accelerated temperature cycle (ATC) testing per IPC-9701, using the 0°C to 100°C temperature cycle range.

Figure 1: Encapsulant Assembly Process

For the control boards, dye and pry techniques in addition to x-sectioning were utilized to validate the inspection results. However, with the encapsulant materials, only x-sectioning is utilized for physical analysis. Since the encapsulant material may inhibit accurate results regarding the solder joint integrity with the use of a dye and pry technique, this was not used for physical analysis of the boards having the encapsulant materials.

TEST VEHICLE

Test vehicle 1 (TV1), shown in Figure 2, was designed to investigate the influence of various design parameters on the solder joint integrity in a mixed VIPPO and non-VIPPO BGA footprint within the PCB for a given set of controlled PCB factors such as PCB thickness (125 mils), material (Megtron 6) and number of stack-up layers (16). This design used the footprint for DDR4 BGA components (13.3 x. 7.5 mm sq., 0.8mm pitch) for this evaluation.

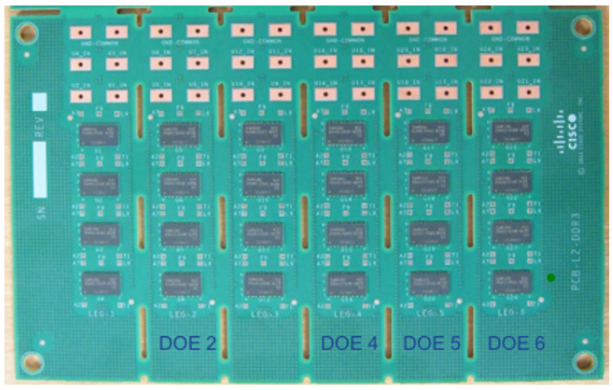

Figure 2: Test Vehicle 1 (TV1)

For TV1 shown above, the package footprint is exhibited in Figure 3 below. Only the locations marked as DOE2, DOE4, DOE5 and DOE6 are populated for the purposes of this evaluation, as these are the locations having a footprint with the PCB design attributes known to induce both of the solder joint assembly defects targeted for this study.

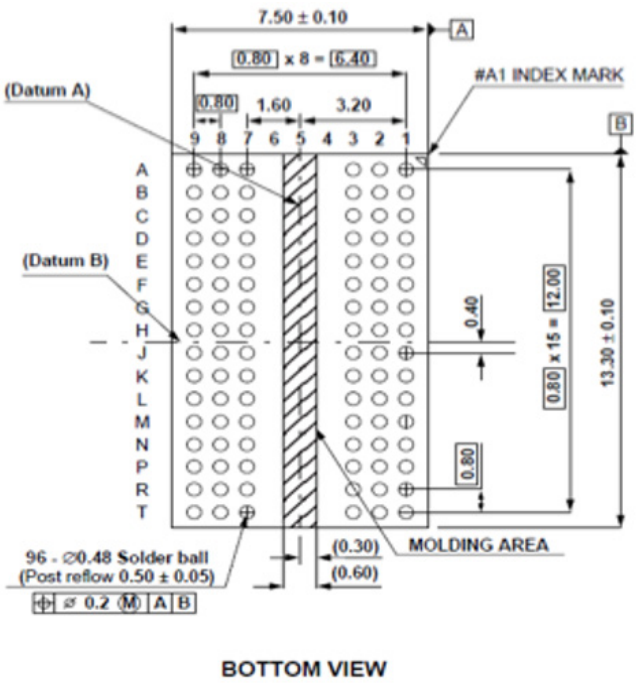

Figure 3: Package Footprint on Test Vehicle 1 (units in mm)

Test vehicle 2 (TV2), shown in Figure 4, includes a variety of fine pitch BGA component sizes and BGA pitches, again having mixed VIPPO and non-VIPPO BGA footprints. This board design includes BGA body sizes, ranging from 10x10 mm sq. up to 37x37 mm sq., and BGA pitches, ranging from 0.7mm to 1.0 mm. Again, the same set of controlled PCB factors as defined in TV1 for thickness, PCB material and stack-up are also employed. Neither test vehicle includes any components on the bottom-side.

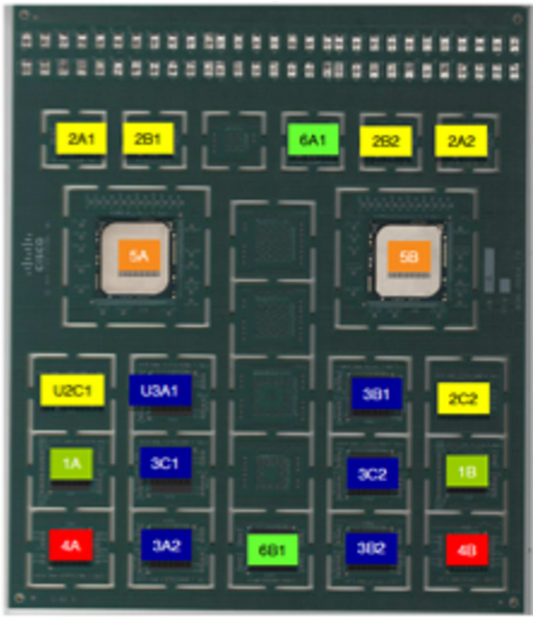

Figure 4: Test Vehicle 2

ASSEMBLY PROCESS

In order to understand the compatibility of these solder joint encapsulant materials with existing standard SMT assembly materials and processes, both test vehicles are assembled with two different production solder pastes and conventional production SMT equipment is used, including solder paste printing, pick and place and reflow. Subsequently, x-ray inspection is performed although digital x-ray tomosynthesis capabilities were not available for this study.

Each test vehicle is assembled and subsequently put through a secondary reflow in order to simulate both a secondary SMT attach process, followed by inspection and physical analysis to validate the solder joint integrity after each reflow. Reflow profiles for both test vehicles are shown in Figures 5a and 5b below. The printed circuit assembly equipment, process parameters, tooling (e.g. stencil design and technology), and assembly materials (e.g. solder paste) utilized for these builds are consistent with standard production processes in order to minimize the number of variables introduced in this study. However, as this assembly was performed in a development lab rather than a production floor, access to the 5DX or equivalent digital x-ray tomosynthesis inspection equipment was not available.

Figure 5a: DDR4 TV Reflow Profile

Figure 5b: Fine Pitch TV Reflow Profile

RESULTS

Assembly

The assembly performance of two solder joint encapsulant materials were compared with control boards having no solder joint encapsulant material for two different test vehicle designs, a DDR4 test board and a fine pitch test board.

As expected, the DDR4 test vehicle, which used a component package previously known to result in HIP defects, was found to

exhibit numerous HIP defects after the initial SMT reflow on the control boards. These HIP defects occurred similarly with both solder pastes and, after the 2nd reflow, these HIP defects were mostly 'healed'. During the secondary reflow, when there is a forced constraint of the package due to the previously formed solder joints, any movement of the package is restricted prior to reflow so that these HIP joints are able to properly coalesce and 'heal' during reflow. After the 2nd reflow, there were, however, significant solder separation defects present on the control boards, again, regardless of solder paste, as shown in Figure 6. Both solder joint encapsulant materials were found to mitigate the solder separation defects on the DDR4 test vehicle as shown in Figure 7, but only the solder joint encapsulant material A, however, was able to mitigate the HIP defects. Extensive solder voiding was also identified with the solder joint encapsulant material B and is illustrated in Figure 9. This voiding was considered to be within IPC workmanship standards, but was marginal in some cases and would require additional process optimization. However, for the purposes of this study, further investigation of this voiding phenomenon was not pursued. The solder joint encapsulant B material also exhibited solder bridging defects as shown in Figure 9, possibly due to inconsistent coverage or voiding of the encapsulant material leading to solder extrusion, and there was significant solder balling both within the BGA array as well as around the periphery of the package, as seen in Figure 8.

For the Fine Pitch test vehicle, the control boards and boards using the solder joint encapsulant B material exhibited solder separation defects after the 2nd reflow, as illustrated in Figure 10. This occurred primarily with one of the solder pastes. Moreover, the boards using the solder joint encapsulant B material again exhibited extensive solder voiding, solder bridging and solder balling as seen in Figure 11. The boards using the solder joint encapsulant A material, however, were shown to mitigate the solder separation defect. These boards did show pronounced solder voiding, as seen in Figure 12, which was within IPC workmanship standards, but, again, marginal in some cases and would require further optimization. Additionally, for the largest package size, the 37.5 mm sq. FCBGA, the solder joint encapsulant A material was found to be uncured underneath the center of the package, even after 2 reflows. Further investigation by the material manufacturer has been pursued to address this issue. Similar results were exhibited with both solder pastes.

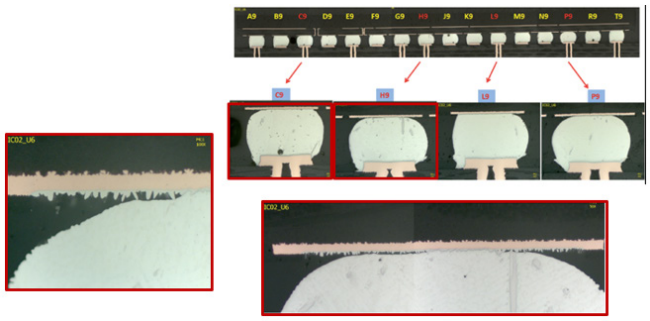

Figure 6: Solder Separation on DDR4 Control Boards

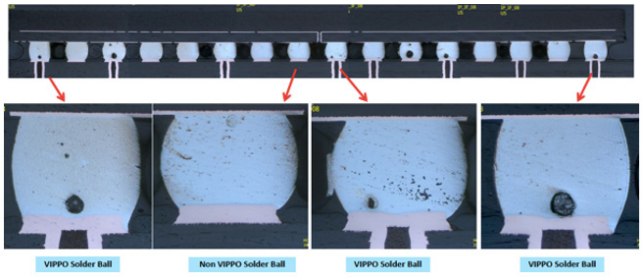

Figure 7: DDR4 TV Assembly Results with Solder Joint Encapsulant Material A

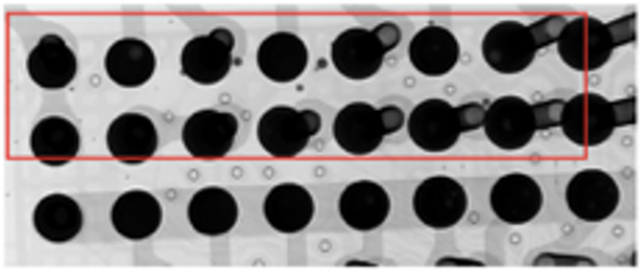

Figure 8: Solder Balling with Solder Joint Encapsulant Material B on DDR4 TV

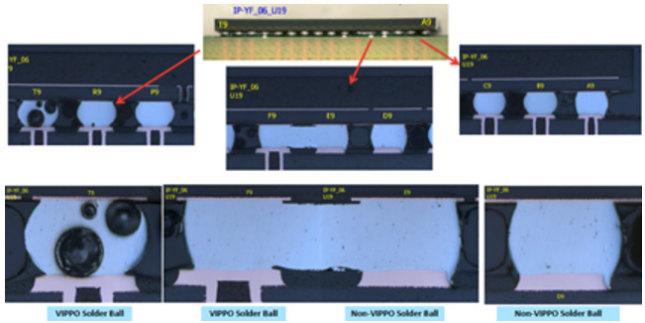

Figure 9: Solder Voiding and Bridging with Solder Joint Encapsulant Material B on DDR4 TV

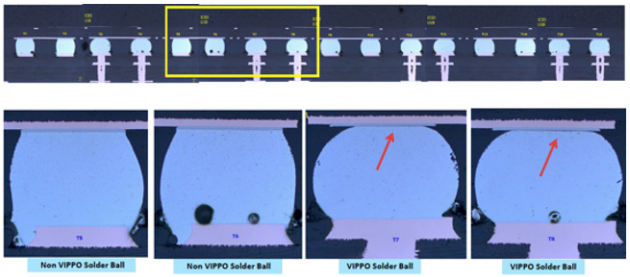

Figure 10: Solder Separation on Fine Pitch TV Control Boards

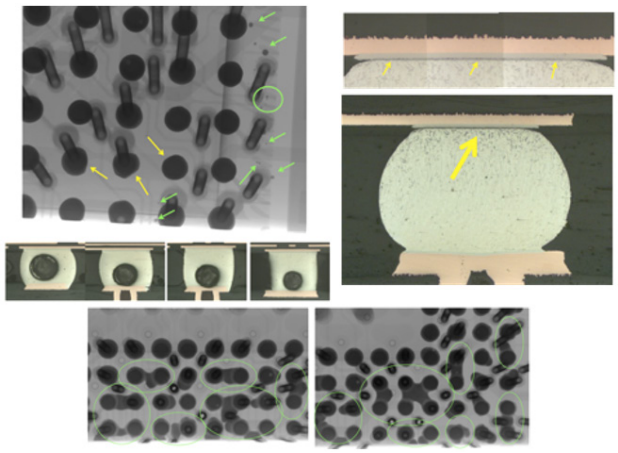

Figure 11: Solder Defects with Solder Joint Encapsulant Material B on Fine Pitch TV Control

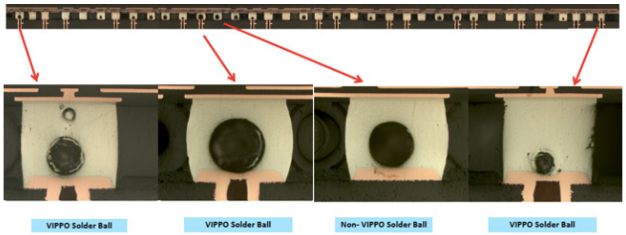

Figure 12: Solder Voiding with Solder Joint Encapsulant Material A on Fine Pitch TV Control

Reliability

The remaining boards for both the DDR4 test vehicle as well as the Fine Pitch test vehicle were submitted for accelerated temperature cycle (ATC) testing per IPC-9701 test conditions of 0°C to 100°C for a minimum of 3500 cycles or 50% failure. The DDR4 test vehicle was assembled with functional parts as daisy-chained components were not available. Therefore, samples of these boards for each of the 3 build legs, control boards with no solder joint encapsulant, boards assembled with solder joint encapsulant material A and boards assembled with solder joint encapsulant material B, were pulled at certain temperature cycle intervals and subjected to physical analysis employing dye and pry or x-section to assess the solder joint integrity. For the Fine Pitch test vehicle, daisy-chained components were available and used for the assembly of these boards. In this case, in-situ resistance monitoring of the daisy-chain nets was utilized to assess the solder joint integrity of each component throughout the ATC testing. The solder joint reliability results for these test vehicles are summarized in Tables 1 and 2.

Table 1: Solder Joint Reliability Comparison for Solder Joint Encapsulant Material A on Fine Pitch TV

Package Type	Control		Solder Paste 1 Solder Joint Encapsulant A		Solder Paste 2 Solder Joint Encapsulant A	
	Beta	Charcteristic Life	Beta	Charcteristic Life	Beta	Charcteristic Life
10mm sq. 0.8mm pitch	*4.7*	*2366*	1.55	754	3.06	1112
15mm sq. 0.8mm pitch	*1.05*	*397*	3.56	445	3.05	649
17mm sq. 1.0mm pitch	0.48	495	3.36	474	1.92	559
19mm sq. 0.8mm pitch	2.76	1077	1.08	648	4.4	625
37mm sq. 0.7mm pitch variable	5.2	1773	*0.7*	*584*	7.41	1537

***Note: Beta < 1 likely due to multiple failure modes (e.g. solder separation defects or assembly defects related to the encapsulant resulting in early failures).**

Table 2: Solder Joint Reliability Comparison for Solder Joint Encapsulant Material B on Fine Pitch TV

Package Type	Control		Solder Paste 1 Solder Joint Encapsulant B		Solder Paste 2 Solder Joint Encapsulant B	
	Beta	Charcteristic Life	Beta	Charcteristic Life	Beta	Charcteristic Life
10mm sq. 0.8mm pitch	*4.7*	*2366*	3.21	1426	2.81	1764
15mm sq. 0.8mm pitch	*1.05*	*397*	4.9	310	0.99	439
17mm sq. 1.0mm pitch	0.48	495	1.7	282	1.13	511
19mm sq. 0.8mm pitch	2.76	1077	7	497	6.01	671
37mm sq. 0.7mm pitch variable	5.2	1773	4.38	1187	3.79	1769

***Note: Beta < 1 likely due to multiple failure modes (e.g. solder separation defects resulting in early failures for control parts).**

The DDR4 test vehicle exhibited similar solder joint reliability among all 3 categories, the control boards with no solder joint encapsulant, boards with solder joint encapsulant material A and boards with solder joint encapsulant material B as well as for both solder pastes. Solder joint crack initiation was identified after 750 cycles with significant solder joint cracking found after 1500 cycles.

The Fine Pitch test vehicle exhibited comparable solder joint reliability between the boards with the solder joint encapsulant materials and the control boards with no solder joint encapsulant material in most cases. Additionally, no specific trend could be identified with the solder paste materials. In a few instances, the characteristic life for a component on the boards with the solder joint encapsulant material(s) was significantly lower than that for the control boards. However, based on initial physical analysis results, it is suspected that assembly defects due to the encapsulant material were likely present for those components which degraded their solder joint reliability. Unfortunately, 5DX inspection or equivalent was not available during the assembly of these test boards and through-scan x-ray data was not retained for reference. Prior to physical analysis with x-sectioning, x-ray inspection was also performed in the FA lab, which identified deformed solder joints and possible solder extrusion through gaps in the coverage of the solder joint encapsulant around the solder joint. Representative images of these possible solder defects are shown in Figures 13 and 14 and representative images of solder joint cracking are presented in Figure 15.

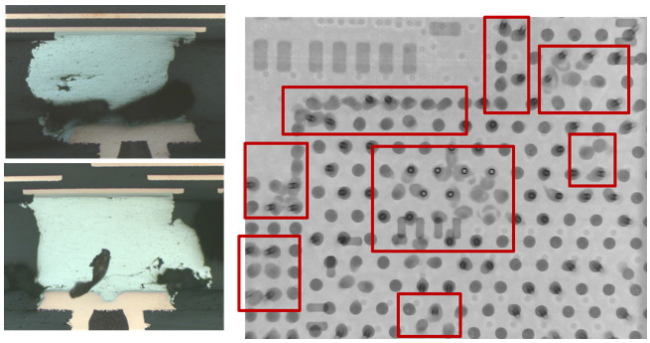

Figure 13: Deformed Solder Joints Found after ATC Testing with Solder Joint Encapsulant Material A

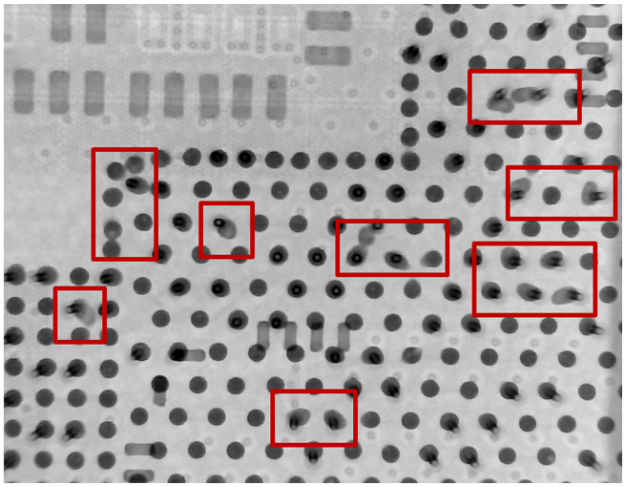

Figure 14: Deformed Solder Joints Found After ATC Testing with Solder Joint Encapsulant Material B

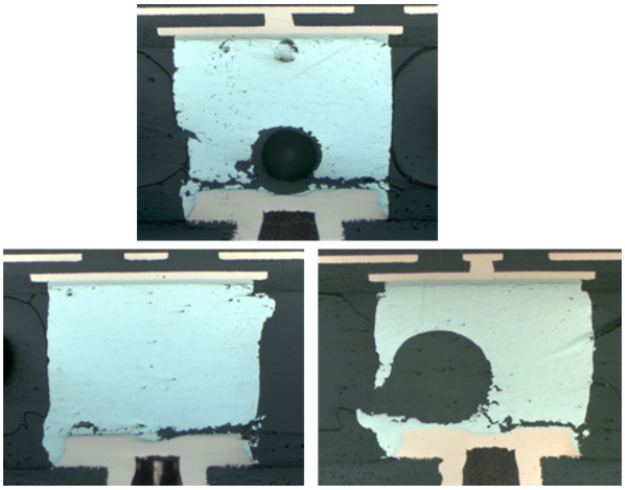

Figure 15: Solder Joint Cracking with Solder Joint Encapsulant Material B After ATC Testing (3500 cycles)

DISCUSSION

This study has shown the solder joint encapsulant material A to be effective in the mitigation of the solder separation defects associated with the use of VIPPO and VIPPO+BD structures within the BGA footprint of a PCB design. This material was also demonstrated to be effective in mitigating HIP defects associated with small, lightweight BGA packages having < 3 mils warpage. These results were consistent across both solder pastes on both test vehicles, as applicable. The solder joint encapsulant material B, however, was found to introduce numerous assembly defects, including solder bridging, deformed solder joints and solder balling, without effectively mitigating either the solder separation defects or the HIP defects. Again, these results were consistent across both solder pastes and both test vehicles. Both solder joint encapsulant materials exhibited significant voiding as compared with the control parts without any solder joint encapsulant. Although the voiding was determined to be within IPC workmanship standards for these test vehicle builds, it was marginal in many instances and may be of concern for a volume production process.

In terms of the influence of these solder joint encapsulant materials on the long-term thermo-mechanical solder joint reliability, initial results from the DDR4 TV suggest that these materials do not have a significant influence on the ATC reliability. For the Fine Pitch TV, which exhibited solder joint defects related to the assembly process with the encapsulant materials, further testing will be needed to characterize the impact of the encapsulant on the solder joint reliability, as there were likely multiple failure modes exhibited in the Weibull distributions. For instance, in the cases showing an appreciable degradation in the characteristic life during ATC testing, the preliminary physical analysis indicates that these early failures are likely due to deformed solder joints resulting from the assembly process rather than conventional solder joint fatigue failures. It is suspected that the volume of the encapsulant material was not consistent across all of the solder joints, possibly due to non-coplanarity of the package, and areas of excessive encapsulant material interfered with proper solder joint formation. The deformed shape of these solder joints does not conform to typical solder joint shapes driven by surface tension. Additional studies should be pursued to further validate this and to investigate further process optimization of the solder joint encapsulant material A to ensure more consistent assembly results.

SUMMARY AND CONCLUSIONS

This work has investigated the assembly performance, defect mitigation effectiveness and influence on long-term solder joint reliability for 2 different solder joint encapsulant materials using 2 different solder pastes. In addition, 2 different test vehicles known to induce the solder separation and HIP defects were utilized in this study, which included control builds without any solder joint encapsulant material and builds with the 2 different solder joint encapsulant materials. In each case, 2 different solder pastes were used in the assembly of each test vehicle.

It was shown that the solder joint encapsulant material A may be a potential solution to mitigate both of the assembly defects

investigated in this study. This material was also demonstrated to be compatible with existing standard production SMT processes. Furthermore, neither solder joint encapsulant material appears to significantly influence the long-term thermo-mechanical solder joint reliability of these packages. However, additional process optimization with the solder joint encapsulant materials would be needed to ensure more uniform solder joint formation for consistent ATC reliability as well as to achieve increased process margins for volume production.

FUTURE WORK

Further development work on the formulation of the solder joint encapsulant material A is being pursued by the material manufacturer to optimize the assembly performance, in terms of the curing behavior and process window. Based on some of the promising results found from this study, future evaluations to characterize the assembly performance of the optimized formulation of this solder joint encapsulant materials may be pursued.

Moreover, since these materials have been shown to provide enhanced adhesion strength for BGA solder joints during SMT reflow, there may be other potential applications for these materials. For instance, the non-wet open defect5 may potentially be mitigated with increased adhesion strength of the solder joint during reflow due to the encapsulant. In addition, as we are seeing increasing usage of bottom-side large body BGA components, particularly with the proliferation of high-speed BGA connectors, the solder surface tension is no longer sufficient to overcome the gravitational force on these components when the board is flipped and put through the top-side reflow process. These solder joint encapsulant materials may prove to be effective in adhering these bottom-side large body BGA components to the board during the top-side reflow process. These potential application areas should be investigated to characterize the effectiveness of these materials in mitigating these other assembly challenges.

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BIOGRAPHIES

Sue Teng is currently a Sr. Manufacturing Engineer at Google leading printed circuit assembly technology development for next-generation machine learning products to support the Google Cloud infrastructure. Prior to joining Google, she was a technical leader at Cisco Systems, most recently within the Global Manufacturing Operations organization responsible for printed circuit assembly technology development for next-generation semiconductor, interconnect and optics packaging. She has also held various roles within the Technology and Quality organization at Cisco Systems, leading ASIC packaging development and reliability qualification activities as well as interconnect technology reliability characterization. She holds a B.S. and M.S. in mechanical engineering from U. C. Berkeley and has extensive experience in microelectronics packaging, including thermal and thermo-mechanical issues, interconnect reliability and substrate technology.

Cherif Guirguis received his BS degree in Mechatronics engineering from Ecole Polytechnique of Montreal, Canada and an MS degree in Engineering management from Santa Clara University.

Cherif has been working at Cisco for 11 years. He was a senior FA engineer that has been part of Material Science and Failure analysis lab since 2011. His primary focus was on FA support for hardware product development, troubleshooting field returns and line stop/stop ship issues. Cherif is currently working as a Senior Optical Component Engineer handling technical assessment of optical suppliers including next generation technologies and packaging solutions. He has also been assessing reliability risk, developing and executing qualification plans and resolving technical issues. Cherif has co-authored over 15 publications and articles and is a member of SMTA.

Gnyaneshwar Ramakrishna, serves as a Technical Leader overseeing component qualification and reliability at Cisco Systems. His experience ranges from high speed packaging, photonics packaging, connectors, power supplies focusing on product delivery over the past 18 years. In addition, he serves as chair for Photonics technical committee in IEEE-EPS. He holds an MBA from Santa Clara University, Master's in Mechanical engineering from Georgia Tech and Bachelors from IIT-Madras.

Hien Ly has worked in the manufacturing engineering sector for over 28 years. He is currently the engineering manager at Jabil, helping to drive new technology innovations. His competencies are supported by a Bachelor of Science Degree in Electrical Engineering, 8 years of industrial engineering experience in Original Equipment Manufacturer (OEM) production, and 20+ years of Surface Mount Technology (SMT) manufacturing experience. His other capabilities include adaptation to new technologies and broad knowledge of mechanical and electronic devices.

He is a member of the Institute of Electrical and Electronics Engineers (IEEE) and was a participant in Technical Committee of IEEE International Reliability Physics Symposium (IRPS). He has also published and co-authored articles in SMT Magazine and presented at SMTA conferences.

In his spare time, he likes to listen to music and play music instruments. He also likes to work on home improvement projects, automotive maintenance, and home electronic equipment.