SMTAnews

& Journal of Surface Mount Technology

Volume 33, Issue 2, 2020

Information updated daily... check smta.org for the most current association news.

SMTAnews

Volume 33, Issue 2, 2020

2020 Charles Hutchins Educational Grant Recipient Announced

SMTA is honored to announce Chidinma Imediegwu, a graduate student at the Georgia Institute of Technology, has been selected as the recipient of the 2020 Charles Hutchins Educational Grant.

The SMTA Grant Committee selected Chidinma's project entitled "Transient Liquid Phase Bonding and the Development of a Cu-Al Binary System Solder Employed for Durable and Thermally Efficient Electronic Packages." She obtained her bachelor's degree in Mechanical Engineering in 2013, and a Master's degree in 2015 from Southern University, Baton Rouge. Following completion of her doctoral program at Georgia Tech, Chidinma plans to leverage her technical and research background working in Surface Mount Technology on the fabrication and reliability assessment of electronic packages.

The Charles Hutchins Educational Grant, co-sponsored by the SMTA and Circuits Assembly magazine, was established in memory of past SMTA president, educator, mentor, and industry colleague, Dr. Charles Hutchins. The $8000 grant has been presented annually since 1998 to a full time graduate-level student pursuing a degree and working on thesis research in electronics assembly, electronics packaging, or a related field.

The award will be presented in person at the 2021 SMTA International Conference.

The SMTA will begin accepting applications for the 2021 Charles Hutchins Educational Grant in early 2021.

Please contact Tamara Shephard with questions: tamara@smta.org or +1-952-920-7682, or visit the website: www.smta.org/page/hutchins-grant

2020 Stromberg Scholarship Recipient Announced

Sabrina M. Rosa-Ortiz, University of South Florida, has been selected as the recipient of the 2020 Joann Stromberg Student Leadership Scholarship.

The SMTA Awards Committee selected Sabrina for her committed leadership in the SMTA. Sabrina is a Ph.D. candidate from the Electrical Engineering Department at the University of South Florida (USF). As part of her research, she was able to develop a patent named "Electrochemical Three-Dimensional Printing and Soldering" in which she studied the hydrogen evolution assisted electroplating as a reliable source to obtain a rapid and lateral copper deposition. She is currently the SMTA USF Student Chapter president for the University of South Florida and is also responsible for bringing back the SMTA USF Student Chapter to the university.

The $3000 JoAnn Stromberg Student Leadership Scholarship, given in honor of the nearly 30 years of service dedicated by former Executive Administrator, JoAnn Stromberg, was established following her retirement in 2015. The purpose of this scholarship is to encourage students to take on more leadership opportunities and strengthen the connection between students and the electronics industry.

The Stromberg Scholarship is awarded annually to a full-time student pursuing a degree in electronics and actively involved in the SMTA.

The award will be presented in person at the 2021 SMTA International Conference.

The nomination period will be available early next year for 2021 candidates.

Please contact Tamara Shephard with questions: tamara@smta.org or +1-952-920-7682, or visit the website: www.smta.org/scholarship

Members of Distinction Award Winners Announced

The SMTA is proud to honor the 2020 "Members of Distinction" award recipients who have shown exceptional dedication to the association and the electronics assembly industry.

The association's highest honor, the Founder's Award, recognizes members who have made exceptional contributions to the industry, as well as support and service to the SMTA. This year, the committee selected Reza Ghaffarian, Ph.D., Jet Propulsion Laboratory, to receive this prestigious award. SMTA and the electronics industry have benefited immensely from Dr. Ghaffarian's research and advocacy in the area of reliability over the years.

The Member of Technical Distinction Award recognizes individuals who have made significant and continuing technical contributions to the association. This year the Awards Committee selected Lenora Clark, ESI Automotive, as the recipient of this award. Lenora has presented numerous technical papers at SMTA conferences, is a member of the SMTA International technical committee, and most recently co-chairs the Additive Electronics TechXchange.

The Excellence in Leadership Award honors members who stand out as strong leaders in the association. The 2020 recipient of this award is Jasbir Bath, Bath Consultancy. Jasbir has been dedicated to the success of the SMTA for over 20 years. He has demonstrated his leadership experience in various roles on the Silicon Valley Chapter leadership team. Jasbir brings an acute attention to detail, inclusivity, and passion for his chapter and to technical knowledge sharing. The SMTA thanks Jasbir for his many valuable years of service.

The Excellence in International Leadership Award recognizes members who have provided outstanding support and leadership to the SMTA's international members, chapters, or educational programs. The recipient selected for this award is Kong Hui Lee, Ph.D., CSMTPE, Cisco Systems (Malaysia) Sdn. Bhd. KH has been instrumental in bringing technical presentations to the SMTA Penang Chapter as well as working with headquarters to bring that information to a global audience.

L3HARRIS Technologies received the SMTA+ Corporate Partnership Award this year. As a global member, L3HARRIS has shown support at every level of the association from supporting chapter leadership positions to technical contributions for conferences, committees, and most importantly their willingness to share technical knowledge with others in the industry. They embody the SMTA mission by encouraging employees to become members, attend meetings and share their knowledge. L3HARRIS is most deserving of this honor.

SMTA has recognized exceptional individual and corporate members for their immeasurable contributions to the association since 1994.

View details at the website:
www.smta.org/page/current-recipients

Please contact Tanya Martin, tanya@smta.org or +1-952-920-7682, with questions.

Additive Electronics TechXchange Free for Members

October 15, 2020

Speakers from major electronics manufacturers and academia will present research as part of the technical program of the Additive Electronics TechXchange on October 15, 2020. Presenting organizations include Auburn University, Duke University, Intel Corporation, Lockheed Martin, Northrop Grumman, and NSWC Crane.

The Additive Electronics TechXchange examines the manufacturing and design processes enabling line width and space from .003" to 5 microns as well as other new advanced technologies intended to meet the ever-increasing challenges of smaller, lighter and more powerful electronic devices. This year the event organizers expect to dive deeper into market trends, usage and where additive fits within low, medium and high-volume production for this portion of manufacture where the electronics industry straddles the line between PCB and IC substrate.

Sponsoring companies include AGC Taconic, American Standard Circuits, Inc., Averatek Corporation, Calumet Electronics Corporation, FTG - Firan Technology Group, Insulectro, MacDermid Alpha Electronics Solutions, and SUSS MicroTec. The conference is supported by Iconnect007.

Registration is free for SMTA members and sponsorship opportunities are available. For full details and to register, visit www.smta.org/additive/ or contact Jaclyn Sarandrea: +1-952-920-7682 or jaclyn@smta.org.

SMTA

EDUCATIONAL OPPORTUNITIES

CONFERENCES

One of the ways SMTA enables its members to achieve professional success is by providing unparalleled educational programs and events all around the world. View our website to see the various opportunities available to you.

CERTIFICATION

Gain the most respected sign of approval in the electronics assembly industry! Each SMTA Certification program is a three-day offering consisting of a 1.5-day workshop on topics in SMT Processes followed by open and closed-book exams.

ONLINE TRAINING

Low-cost, self-paced, online training on electronics manufacturing fundamentals. Courses currently available; Stencil Printing, Component Placement, Reflow Soldering, Wave Soldering, Selective Soldering, Rework, and Cleaning.

WEBINARS

Listen to outstanding speakers without leaving your desk! SMTA Webinars are a great solution for getting the latest information on electronics assembly and advanced packaging at the best price. View all upcoming webinars online.

www.smta.org

IWLPC Panel Addresses Future Packaging Challenges

October 14, 2020 @ 9:00am US Pacific Time | On-Demand Playback Available

The International Wafer-Level Packaging Conference and Expo announces a panel discussion titled "Meeting Future Advanced Packaging Challenges: What's Next?" The live discussion will commence on Wednesday, October 14, 2020 at 9:00am US Pacific Time.

The panel will discuss challenges and possible solutions to advancements in heterogeneous integration, high density substrates, and Fan-Out Wafer-Level Packaging (FO-WLP) as they impact material selection, design and fabrication of features, inspection, test, and reliability. Attendees will be able to submit questions and get responses in real-time from the expert panel.

Panelists include Tim Olson, DECA; Tanja Braun, Ph.D., Fraunhofer IZM; Rahul Manepalli, Ph.D., Intel Corporation; Max Min, Ph.D., Samsung Foundry; and Shin-Puu Jeng, Ph.D., TSMC. The panel is moderated by E. Jan Vardaman, TechSearch International, Inc.

The panel discussion is open to all registered attendees. The technical conference and expo are available on-demand from October 13-30 with a live, online exposition enabled October 13 and 14.

For questions about IWLPC, please contact Jaclyn Sarandrea, jaclyn@smta.org or visit www.iwlpc.com.

SMTA International On-Demand Until October 23, 2020

SMTA International kicked off September 28, 2020 as a completely virtual event.

The live days may be over but don't let that stop you from watching on-demand technical presentations and exploring the virtual exhibit hall at SMTA International! Conference attendees will have access to the on-demand presentations and the exhibit hall will be open to everyone until October 23. Watch and even re-watch pre-recorded technical presentations all available at your fingertips.

Several professional development courses are still available for registration through the end of the conference. Those topics include Defect Analysis and Process Troubleshooting: Part 1 & 2, Tips and Tricks for Cleaning Circuit Assemblies, Design and Assembly Process Challenges for Bottom Terminations Components, and Principles and Practice of Developing Soldering Profiles.

Further details about SMTA International conference and exhibition are available online at www.smta.org/smtai.

Still Accepting Abstracts for Pan Pac

The Pan Pacific Microelectronics Symposium is scheduled for February 1-4, 2021 in Honolulu, Hawaii. The Program Committee invites you to submit your recent results for presentation at the Symposium. Abstracts of 500 words should be submitted with title and author contact information. Let us know if you want an official letter in support of management approval for your paper submission.

Full technical papers are required for conference participation. Papers should be 6-10 pages in length including graphics, and they should offer non-commercial research results on any of the topics listed below.

You will be notified by November 2020 if your abstract has been accepted and scheduled for presentation. All accepted papers will be published in the conference proceedings, SMTA Knowledge Base and submitted to the IEEE Xplore Digital Library.

For details, visit www.smta.org/panpac or contact Karlie Severinson by email at karlie@smta.org or by phone at +1-952-920-7682.

SMTA International

Conference: November 1 - 4, 2021
Exposition: November 3 - 4, 2021

Minneapolis Convention Center
Minneapolis, MN, USA

**Co-located with MD&M Minneapolis*

CALL FOR abstracts

The SMTA invites you to submit an abstract for the annual SMTA International Conference. Share your research and be part of the industry's strongest technical program. Full technical paper is required.

Proposals are also being solicited from individuals interested in teaching professional development courses related to surface mount technology, advanced packaging, and electronics manufacturing.

SMTA International Offers Five Awards

Best of Conference Presentation ($1,000 USD)
1st Place Best of Proceedings Paper ($1,000 USD)
2nd Place Best of Proceedings Paper ($500 USD)
3rd Place Best of Proceedings Paper ($500 USD)
Best Student Presentation ($500 USD)

www.smta.org/smtai

Due Date: March 1, 2021

Journal of Surface Mount Technology
October 2020 | Volume 33, Issue 2
ISSN: 1093-7358

6600 City W Parkway, Suite 300
Eden Prairie, MN 55344, USA

Phone: +1 952-920-7682
journal@smta.org
www.smta.org

COMMITTEE MISSION STATEMENT

The mission of the SMTA Journal Committee is to select and review papers for publication in the Journal of SMT, ensuring a high standard of quality for each issue and ensuring article content best serves SMTA membership.

Friends, hello from the editorial desk. We all at SMTA, and journal review committee hope that all of you and yours are staying safe and healthy. The COVID-19 pandemic did put a glitch in our face-to-face meetings for SMTAI, but still has not dented our spirits of learning and technology as we are meeting for SMTAI virtually. This is the second and penultimate issue for the year 2020 and we hope to give you one more before we close out this fateful year.

I implore all authors to follow the step by step procedure below for instructions on how to get an account on the open access system, submit your paper, and access the reviews on-line. For any queries you might have, contact Ryan Flaherty (ryan@smta.org).

As always, we are bringing three great technical papers in this issue. In the first paper, how conformal coating stresses the WLCSP is studied under conditions of thermal cycling. Next, we focus on enhancing the productivity of plating on PCBs using periodic pulse plating technique. The final paper discusses the effects of multi-axial loading on performance of WLCSP during thermal cycling.

To submit your original papers to the Journal of SMT, please follow the instructions provided below and send any questions via e-mail to ryan@smta.org.

— *Srini Chada, Ph.D.*
The Journal of SMT Editor/Journal Committee Chair

SUBMIT ORIGINAL PAPERS FOR REVIEW:

1. Go to **https://journal.smta.org** and click "Register"
2. Complete the form to create your profile in the system
3. Once your profile is active, click "Make a Submission"
4. Read all requirements and begin the 5-step process:
    a. Acknowledge and accept the requirements
    b. Upload your paper
    c. Enter metadata
    d. Confirm your submission
    e. Review next steps of the process

Contact Ryan Flaherty with questions: ryan@smta.org

ABOUT THE JOURNAL OF SMT

The Journal of SMT is a quarterly, peer-reviewed, technical publication of articles related to electronic assembly technologies, including microsystems, emerging technologies, and related business operations.

IMPACT OF CONFORMAL COATING INDUCED STRESS ON WAFER LEVEL CHIP SCALE PACKAGE THERMAL CYCLING PERFORMANCE

[1]Andy Hsiao, [1]Mohamed Sheikh, [2]Karl Loh, [2]Edward Ibe, and [1]Tae-Kyu Lee
[1]Portland State University, Portland, OR
[2]Zymet, East Hanover, NY

ABSTRACT

Conformal coating is commonly used for harsh environment to protect electronics from moisture and chemical contaminants. But the stresses imparted by the conformal coating can cause degradation to the package thermal cycle performance. Full coverage of the component with conformal coating material can prevent potential corrosion induced degradation but imply a local compression stress during thermal cycling, resulting a different thermal cycling performance compared to non-coated components. In this study, 8x8mm^2 wafer level chip scale packages (WLCSP) were subjected to 5% NaCl aqueous spray test with and without full conformal coating, then thermal cycled from -40ºC to +125ºC. Weibull reliability statistics indicated that fully conformal coated components experience characteristic life cycle number reduction from 404 cycles to 307 cycles, a 24% lifetime reduction, comparing to no conformal coated, no salt spray test applied components. The correlation between crack propagation and localized recrystallization were compared in a series of cross section analyses using polarized imaging and electro-backscattered diffraction (EBSD), which revealed that the conformal coating induced a z-axis tension and compression strain during thermal cycling, resulting in an accelerated degradation at the solder interconnect. Linear Laser profilometer measurements showed that fully conformal coated samples experienced a higher z-axis height displacement change relative to non-conformal coated samples when exposed to 125°C with 10 minutes dwell. To prevent this z-axis strain a reworkable edgebond adhesive was applied with full conformal coating configuration, which demonstrate an increase of characteristic lifecycle number to 2783 cycles, suggesting that the mitigation of the z-axis strain can vastly enhance the thermal cycling performance.

Keywords: WLCSP, Conformal coating, thermal cycling, microstructure

INTRODUCTION

The need for corrosion resistance performance in electronic devices and components become more important with emerging applications in wide range of environments subjected to a diverse array of extreme conditions [1-3]. The amount of data concerning the corrosion properties of electronic products are continuously growing. It is well established that tin-based interconnections like solder joints are less problematic subjected to corrosion because of their relatively strong corrosion resistance.[4-6] It has been reported that the main component of solder alloys, tin (Sn), resists corrosion because of the passivity of the film that forms on its surface [7,8]. The results of various studies show that Sn–3.0Ag–0.5Cu (wt%) (SAC305) solder exhibits better corrosion resistance than other Sn-based alloy compositions due to its high content of noble or inert elements (Ag and Cu) and its stable structure [7,9]. But in earlier publication, it was also shown that the existence of Cu_6Sn_5 and Ag_3Sn intermetallic precipitates in the solder provided unique conditions to the solder joint corrosion mechanism [4,10]. These intermetallic precipitates, in addition to functioning as noble materials, also form galvanic couples with the Sn. Even though the NaCl condition did not affect the whole Sn based solder joint, a localized reaction can degrade the joint stability. Also the NaCl solution did not degrade all solder joints but affected selected joints which are preferred in grain orientation [10]. Figure 1 shows the correlation between the corrosion path and the c-axis direction of the Sn lattice after solder joints after 5% NaCl test. It revealed that the Corrosion path affected by just a small portion of corrosion region at the initiation point then with crack propagation followed and aligned with the Sn lattice basal plane [10]. Given this example, even if the overall solder joint did not experience severe corrosion, it shows that the joint can suffer accelerated thermal fatigue crack initiation due to the brittle nature of the oxide phase at the stress concentration point. Thus, preventing such localized corrosion in Sn based solder need a full protection from corrosive solutions.

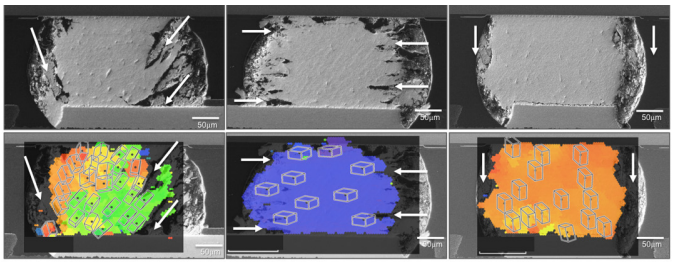

Figure 1. SEM images and OIM maps for 5% NaCl preconditioned joints showing how the corrosion attack is correlated with the Sn lattice basal planes. White arrows indicates the corrosion path [10].

Methods have been made to mitigate corrosive environment exposure to solder joints, using such solutions as conformal coatings. Systematic and in-depth studies had been reported and are still on going on protecting the systems and devices from external environmental risks, like corrosion, and their impact

to the component thermo-mechanical reliability were studied in various aspects [11-19]. Chen et.al reported the impact of conformal coating on BGA components under thermal cycling, vibration and drop test conditions and explained the correlation with the strain rate [13]. Yin et.al performed a study on conformal coated QFN components and reported that the coating reduce stress/strain in solder interconnects and constrains the out-of-plane deformation, which provided both positive and negative impact to the joint reliability [14]. It was also addressed that the level of coating material penetration under the component is an important consideration factor, which was also explained and analyzed in the publication by Serebreni et.al. [15]. Due to the coefficient of thermal expansion (CTE) mismatch, the loading condition per interconnect with and without conformal coating is often an important consideration factor. Detailed studies by Qi et.al and Tong et.al explore effects of the coating material thermo-mechanical behavior on PBGA and Ceramic packages, respectively, and addressed the coating material induced stress and strain impact [16,17]. Studies also reported conformal coating mitigating internally initiated defect risk, like Sn whisker, which can originate from the interconnect region towards outside, causing unexpected electrical shorts [18]. Overall, conformal coatings provide an effective approach of simple protection applied over board components in order to shield corrosion-prone electronic components from exposure. Various types of conformal coating polymer are offered commercially. These include acrylic, epoxy, urethane, silicone resin, and parlyne coatings with various mixed coating materials [19]. But as various earlier publications addressed, the stress and strain, induced from the coating material base properties, layer thickness and penetration under the component, are important consideration factors for a long-term reliability component interconnection. The study presented here is focused on the identification of the conformal coating layer induced strain and stress in the solder joints with various coating thickness, and to identify the effect of restriction of the loading conditions induced by the coating material with the combination of conformal coating and edgebond. A commercial ultra violet (UV) curable acrylated polyurethane conformal coating material was used in this study on 8x8mm² WLCSP components to effectively mitigate localized corrosion due to NaCl reaction. Spray coating applied partially coated components are compared to fully covered conformal coating configuration components, which variations are presented schematically in Figure 2. Ultra violet curing was performed using chemical reaction in the presence of high intensity UV light. A combination of edgebond and full covered conformal coating was tested to see a possible solution to enhance the thermal cycling performance. The extent of degradation, its microstructural evolution and possible mechanisms are discussed. To identify the strain and stress state per solder interconnect, electron backscattered diffraction (EBSD) analysis was performed using strain contour mapping and grain reference orientation deviation maps (GROD).

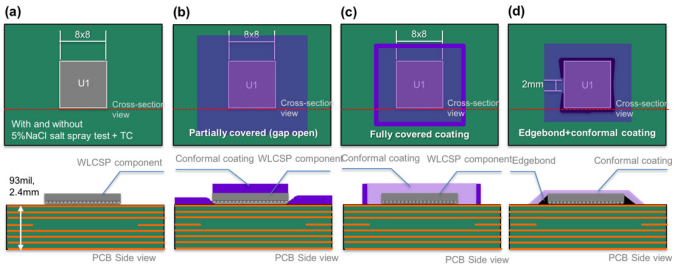

Figure 2. A schematic diagram of the WLCSP sample configurations. (a) assembled WLCSP without conformal coating, (b) Spray conformal coating applied sample configuration, (c) Fully conformal coated sample configuration and (d) Full edgebond with full conformal coating applied configuration.

EXPERIMENTAL PROCEDURE

Body size of 8x8mm², 0.4mm pitch wafer level chip scale package (WLCSP) with 250μm diameter Sn-4.0Ag-0.5Cu (wt%) (SAC405) solder balls were used in this study. A schematic diagram of the WLCSP sample configuration is shown in Figure 3. The parts were board-assembled on 2.4mm (93mil) high glass transition temperature (T_g), FR4-printed circuit boards with OSP surface finishes with a thermal profile of peak temperatures of 240°C, 60 seconds above the liquidus temperature. All components were assembled with SAC305 no-clean solder paste.

For conformal coating, UV curable acrylated polyurethane was used. The glass transition temperature (T_g) of the conformal coating material is -1°C with a coefficient of thermal expansion (CTE) of 122ppm/°C and 264ppm/°C, below and above the T_g, respectively. The coating was applied with spray coating process, which covered the whole PCB but remained partially open between the WLCSP edge and the PCB surface. As schematically shown in Figure 2(b), this allowed a small amount of NaCl solution to penetrate during salt spray testing. To prevent any open gap, the second configuration, a conformal coating dam was built around each component and filled with the conformal coating material to have a fully covered configuration (Figure 2(c)). The additional configuration with the combination of edgebond and conformal coating is presented in Figure 2(d). First, a reworkable edgebond adhesive was selected, which has a T_g of 130°C and a CTE of 30ppm/°C. To prevent voiding due to moisture releasing from PCB material during the curing cycle, test boards are pre-baked for 4 hours at 125°C. The edgebond adhesives were dispensed at room temperature using a pneumatic, hand-held dispenser. The board was then cured at 150°C for 30 minutes. The edgebond adhesive covered three full edges and one side-edge partially opened as indicated as an arrow in Figure 2(d).

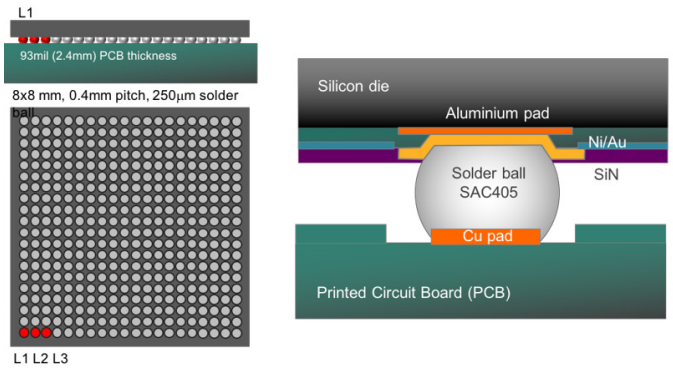

Figure 3. Wafer Level Chip Scale Package (WLCSP) Test component schematic configuration.

After assembly, all the test boards were treated in a salt spray environment with 5% sodium chloride (NaCl) aqua solution (or fog) at 35°C for 150 hours in an enclosed chamber. The salt spray test was performed based on the ASTM B117-09 standard but with an extended holding time for 150 hours instead of 96 hours. After the salt spray test, salt deposits were removed by a gentle rinse of deionized water at room temperature and dried in a dry chamber. For thermal cycling, samples were cycled from -40 to 125 °C at a ramp rate of 10°C per minute with 10 minutes of dwell time. A continuous resistivity measurement using data loggers was applied for each channel with in-situ monitoring during the test. The failure criterion in this study was based on the JESD22-A104D standard, a 20% increase of the peak resistivity for continuous five cycles relative to the initial value. Thermal cycling results for each condition were plotted as Weibull distribution plots.

Laser profilometer measurements were performed using a high accuracy linear displacement sensor (Keyence LK-H022) with a spot size of 25µm at reference distance of 20mm in conjunction with a heating stage designed for minimum z-axis movement during heating as shown in Figure 4. The heating stage was placed on a stepper motorized X-Y-Z stage. The laser sensor was protected from thermal effects with reflective shielding to maintain the operating temperatures of under 50 °C. Each Laser profilometer measurements were conducted at room temperature and 125 °C. As shown in Figure 4(a), each silicon die corner 0.5mm from the edge were measured for linear z-axis height comparison. For Full conformal coated samples, 0.5mm diameter drill holes are applied to measure the Si die top with the 25µm laser spot size.

Cross-sectional analysis using optical microscope with bright light and polarized light were applied to observe the evolution of the microstructures and the locations of the solder joint cracks. Electron microscopy and electron backscatter diffraction (EBSD) analysis was performed with a FEI Sirion FEG-SEM using oxford Instruments high speed EBSD detector. Oxford Aztec and Channel5 Tango software were used to index electron diffraction patterns and analyze collected EBSD data for grain boundary, inverse pole figure, strain contouring maps and grain reference orientation deviation (GROD) maps.

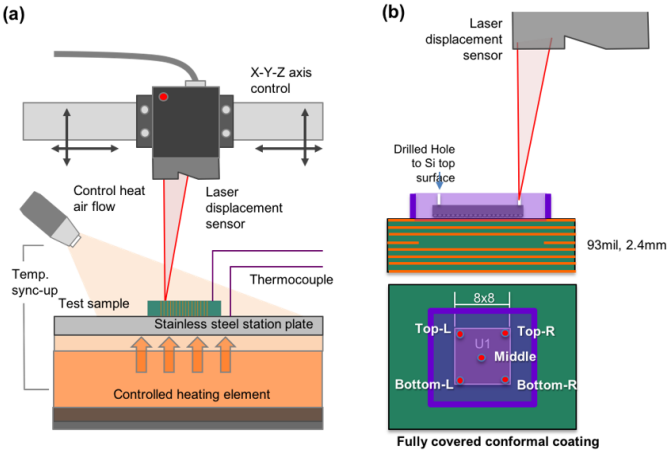

Figure 4. (a) Linear Laser height measurement schematic set-up and (b) sample laser measurement location.

RESULTS AND DISCUSSION

Figure 5 presents the Weibull plots of the thermal cycling results per sample configuration. The sample configuration without conformal coating, not treated with 5% NaCl shows a characteristic life cycle number of 404 cycles with a first failure at 354 cycles, where characteristic life cycle number is the cycle number at 63.5% failure rate. Compared to this baseline data set, the 5% NaCl salt spray treated samples show a characteristic life cycle number as 361 cycles, a small degradation of 10%. But comparing the first failure cycle between those two sample configurations, the cycle number for the NaCl salt spray treated sample component is 232 cycles compared to the no-NaCl treated samples, which is a significant 34% degradation. This can be explained by the corrosion mechanism, which do not affect all solder joint with an overall corrosion rate, but affects selected solder joint with preferred grain orientation, which are exposed to NaCl solution. Because of this, early impacted solder joints show localized corrosion areas causing earlier crack initiation, which led to shorter life cycle numbers. Compared to the no-coated samples, partially coated samples after NaCl treatment (Figure 2(b)), reveal a characteristic life cycle number of 367 cycles, which is similar to the NaCl salt spray treated samples. Also the first failure cycle number is similar with 276 cycles, compared to the NaCl treated samples without coating, which is only a marginal increase. This indicates that the coating layer provided little to no protection to the BGA joints, which is relatively obvious since there is an open gap between the WLCSP component edge and the PCB, so the NaCl solution can penetrate and cause damage to the BGA solder interconnects. Even though the penetration of NaCl solution is expected to be minimal, it can affect preferred Sn grain orientations and initiate the crack propagation.

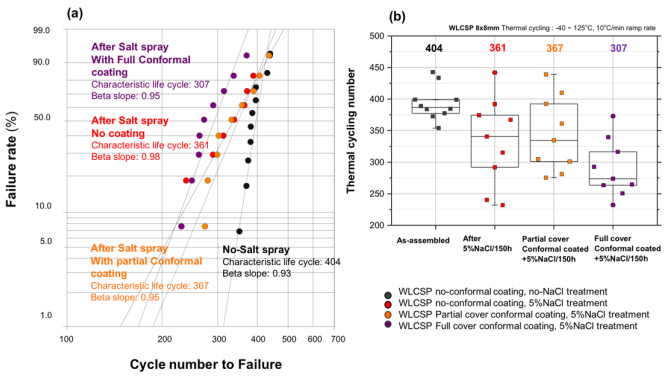

Figure 5. (a) Thermal cycling result Weibull distribution plot and (b) Thermal cycling Failure cycle number distribution plot per sample configuration and post-conditions.

Figure 6 shows the thermal cycled to failure corner solder joints per no-coating and partial coated components after NaCl treatment. As shown in Figure 6(a), as indicated in white boxes, corroded regions are observed at the surface of the solder joints and at the crack initiation region. The corner solder joint with partial conformal coating also show corroded regions at the surface and near the solder to package interface area, which accelerated the crack initiation, resulting in an accelerated crack propagation to failure. Unlike the partially coated samples, the fully coated samples did not show any evidence of NaCl solution penetration and corrosion reaction. But the characteristic lifecycle number is 307 cycles, which is even lower than the NaCl salt spray treated WLCSPs without any protection coating. Since it did not show any corrosion reaction at the BGA solder joints, the degradation seems to be caused by other factors, potentially by the conformal coating induced strain and stress. The cross section and SEM images are shown in Figure 7, comparing the no coating, no NaCl treated sample thermal cycled to failure sample to full conformal coated then thermal cycled sample solder joints. Each sample corner and two adjacent solder joints are selected and shown. Although all solder joints shown full crack propagation near the package side interface region, the non-coated WLCSP, after thermal cycling, exhibits crack propagation with a visually identifiable wide crack opening (Figure 7(a-c)). For the fully coated sample, after thermal cycling, Figure 7(d-f), the crack propagation is observed in a very tight and closed penetration path, which suggests that a compression stress was applied during the thermal cycling process. The height measurement between the package side interface and the board side Cu pad to solder interface before and after thermal cycling on fully conformal coated samples are shown in Figure 8 along with the no coated sample solder heights. As indicated in the full first row solder joints height distribution, a significant reduction of the solder height is identified.

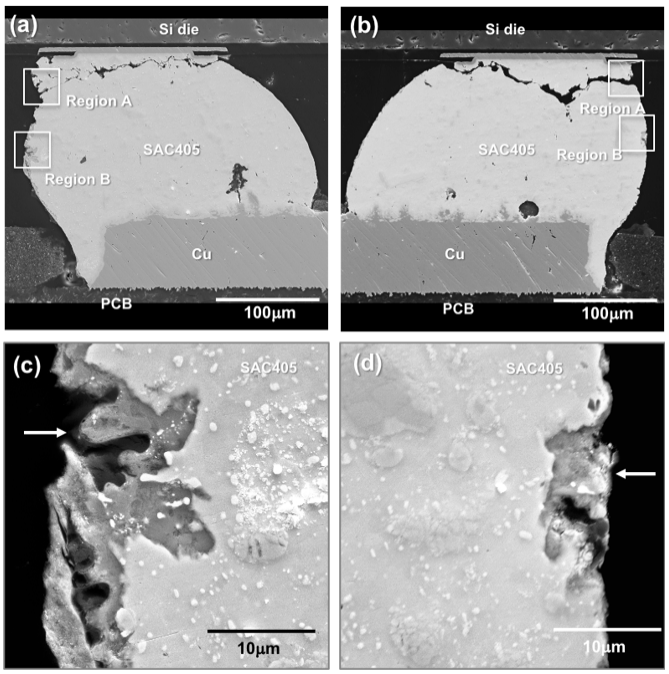

Figure 6. Scanning Electron microscopy (SEM) images on (a) (c) No conformal coating applied WLCSP and (b)(d) Partially conformal coated WLCSP after 5% NaCl spray test for 150h then thermal cycled to failure. Region A and B in (a) and (b) indicates the corroded region. (c) and (d) are higher magnification areas from Region B in (a) and (b). White arrows in (c) and (d)indicates the corroded regions.

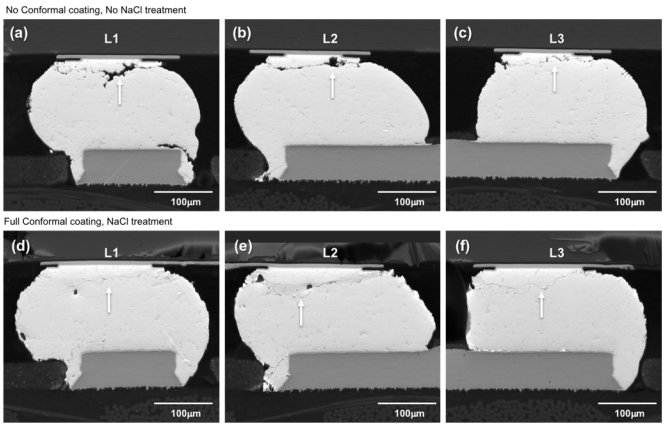

Figure 7. Scanning Electron Microscopy (SEM) images. (a) (b)(c) No conformal coating and no NaCl treatment applied WLCSP thermal cycled to failure,. (d)(e)(f) Full conformal coated samples after 5% NaCl spray test for 150h then thermal cycled to failure. Solder joint location indicated in Figure 2. (a)(d) corner solder joint, L1, (b)(e) L2 and (c)(f) L3. White arrows indicates the crack location.

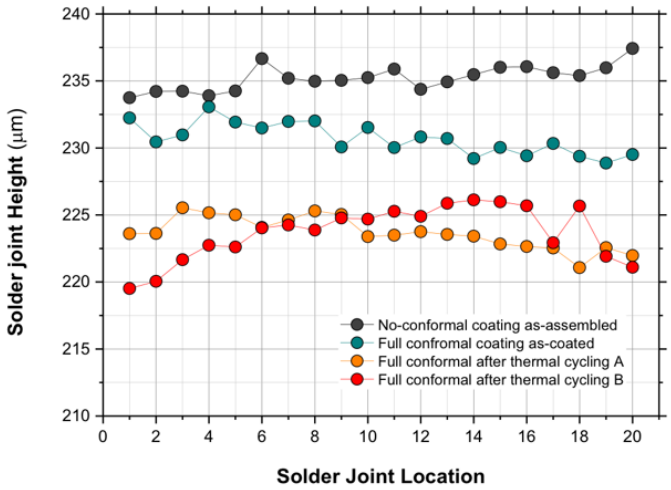

Figure 8. Solder joint height variation per component configuration and thermal cycling.

The reason for the height reduction induced constant compression strain, during thermal cycling can be explained from the component cross-section shown in Figure 9. The coating dam surrounded the WLCSP and the conformal coating material was applied to fill inside the dam to have a full conformal coating configuration. The overall thickness of the conformal coating is 1.3mm, which is 380μm on top of the WLCSP component top surface. Even though this coating is not optimized for best practice, since thinner coating layer is preferred, the coating provided a high level of corrosion protection. Volume shrinkage of the conformal coating materials with long term elevated temperature exposure potentially affected the solder height during thermal cycling, which apply compression stress and strain to the solder interconnects. But the reduction in solder height and compression strain cannot be the dominant factor for the shorter characteristic life cycle numbers, since compression strain to each solder joint actually enhance the solder stability and mitigate the crack initiation and propagation and, should actually result in a longer lifecycle performance, which contradicts the results shown in Figure 5. To identify any possible factor, a linear laser height measurement was applied to Fully conformal coated WLCSPs comparing the height at room temperature and at 125°C. The measurement locations are indicated in Figure 4(a) and the results are shown in Figure 10.

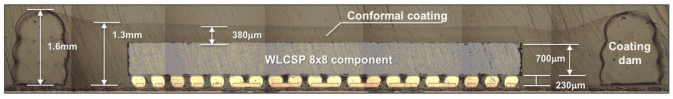

Figure 9. Fully conformal coated WLCSP side view cross section optical image

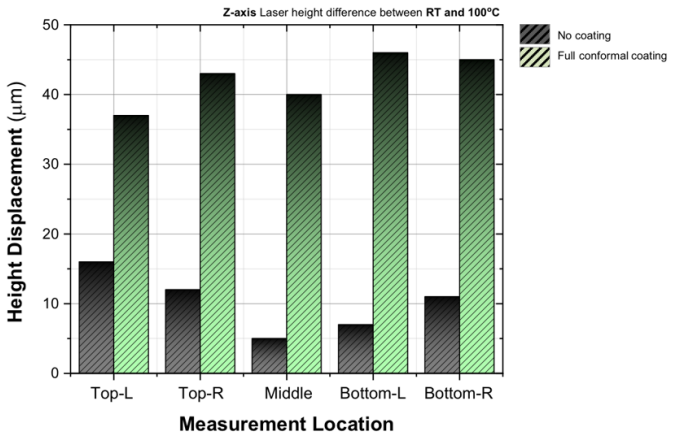

Figure 10. Linear Laser height displacement measurement comparison between room temperature and 125oC for no conformal coated WLCSP and fully conformal coated WLCSP. Laser measurement location are indicated in Figure 4(b).

The height difference between room temperature and 125°C for no conformal coated WLCSP are in the range of 6μm (middle) to 16μm (top left corner). Relative to the middle point, the corner region show a slightly higher height difference. But for the fully conformal coated sample, the Si die surface height difference indicated a 37μm (top left) to 47μm (bottom left) rage of displacement at 125°C, which confirms that the at higher temperature a tension strain induced and negatively affects the stability of the solder joints in fully coated components. The electron backscattered diffraction (EBSD) analysis also revealed the straining in fully coated component solder joint as shown in Figure 11. Three solder joints per no coated and fully coated components shown in Figure 7 are EBSD scanned and each inverse pole figure (IPF), strain contour and grain reference orientation deviation (GROD) maps are compared. Based on the IPF images in Figure 11(a), the no coated component solder joints maintained their single to dual grain structures and developed localized fine grain and recrystallized structure near the package side interface where crack propagation occur. Compared to fully coated component solder joints in Figure 11(b), an overall fully distributed grain refinement is observed with a dominant refinement in L1 joint. The associated strain contour maps revealed a well distributed high level of strain, which can be compared to the low level of strain distribution in no coating applied component solder joints. The strain contour map is converted from scanned EBSD information based on local misorientation and can identify the localized grain region, which measures the level of deviation from the theoretical, non-strained lattice, revealing a distribution map of relatively higher plastic deformation regions [20]. The GROD map in comparison reveals indirectly the relative residual stress level compared to the adjacent grain, by revealing the level of tilting per individual grain compared to a grain orientation reference [20]. Comparing the two EBSD scanning based information conversion, the relative

level of strain and stress for each solder joint can be analyzed. In Figure 11(a) the L1 joint has an overall lower level of strain but localized strain is detected near the package side interface with a relatively high residual stress. But compared to the no coated component L1 joint, the L1 joint in the fully coated component, reveal a full solder high strain level with less residual stress, which means it experience not only a shearing but also an overall tension and compression in the Z-axis direction.

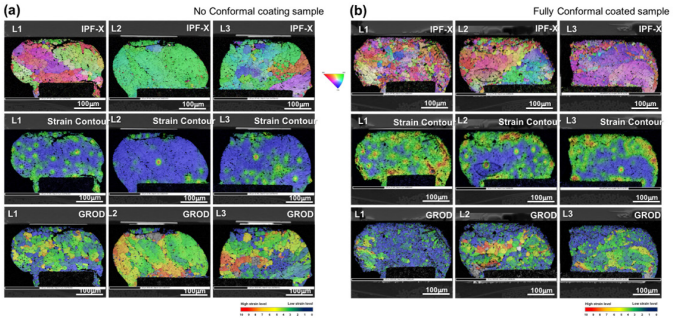

Figure 11. Electron Backscattered Diffraction (EBSD) images for (a) No conformal coated WLCSP after thermal cycling to failure and (b) Fully conformal coated WLCSP after 5% NaCl salt spray test and thermal cycling to failure. The SEM images for L1 to L3 solder joints per sample configuration are shown in Figure 7. Top row is the inverse pole figure (IPF) images, the middle row is the strain contour map, and the bottom row is the Grain reference orientation deviation map.

The EBSD analysis comparison results of these two solder joints, aligned with the laser measurement result and the crack opening comparison in Figure 7. Increased lattice strain in fully conformal coated sample alludes to increased applied strains to the joint by the addition of conformal coating. Recrystallization due to stress relaxation during thermal cycling results in the observed reduction in grain size across the failed joints. The joints from the conformal coated samples revealed increased distribution of recrystallized area per solder joint, which is observed across a majority of the solder joints. This is due to an increased magnitude of thermo-mechanical strain applied by the conformal coating on the joints through large CTE mismatch between the component and PCB. For non-conformal coated samples, recrystallized section of the joints are more localized within the joint, indicating less thermo-mechanically induced strains during thermal cycling. Examining the conformal coating material, the conformal coating shares characteristics of a coefficient of thermal expansion (CTE) of 264 ppm/ °C above a glass transition temperature of -1°C. Compared to average FR4 values of 16-20 ppm/ °C and a glass transition temperature of 135°C. These characteristics indicates that the conformal coating has a greater displacement change with temperature than the FR4 PCB material. Strains generated by the conformal coating on the solder joints are expected with this CTE mismatch between the package assembly and the conformal coating. To find a possible solution to the corrosion and mechanical stress driven degradation, a combination of edgebond and conformal coating was considered and tested. As shown in Figure 2(d), a reworkable edgebond material was applied before conformal coating. The coating covered the edgebond, which closed the gap between the WLCSP and the PCB. Thermal cycling results are shown in Figure 12. The Weibull plot depicts the reliability of the fully conformal coated WLCSP against the edgebond with conformal coated WLCSP. Characteristic life cycle numbers of the edgebond with conformal coated WLCSP was 2784 cycles. The use of edgebond in conjunction with a spray-on conformal coating improved thermal cycling characteristic life by 909% compared to a full conformal coated sample, and 588% improvement over non-coated WLCSP exposed to 150 hr 5% NaCl salt spray test. First failure cycle number was also improved by a similar margin.

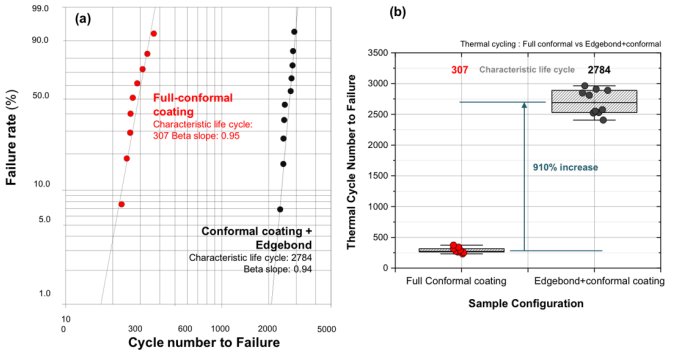

Figure 12. Comparing Fully conformal coated WLCSP with and without Edgebond (a) Thermal cycling result Weibull distribution plot and (b) Thermal cycling Failure cycle number distribution plot per sample configuration.

The mechanical and thermal performance enhancement using edgebond adhesive was studies in various applications [21-24]. Securing the corner and edge without affecting the solder BGA often resulted in an vast improvement in dynamic shock and bend conditions, and with the right combination of T_g and CTE the adhesive improves the thermal cycling performance in both small components like WLCSPs and large components like FCBGAs [21,24]. The main role of these edgebond adhesive is the mitigation of the thermo-mechanically induced strain at the corner and edge region of the component, which resulted in a more stable structure. The combination of edgebonding and conformal coating, which is presented here, provided the enhancement of the thermal cycling performance by restricting the conformal coating induced strain, identified via z-axis height measurement and microstructure EBSD analysis. Thus, the combination of edgebond and conformal coating provides both corrosion resistance and enhanced thermo-mechanical stability to the component.

CONCLUSION

Every day integration of electronic devices requires corrosion resistant methods to be employed in order to maintain device reliability. With this in mind, industry offerings of conformal

coatings provide an option to fulfill that requirement. Conformal coating application methods must be taken into consideration when choosing the method of applying conformal coatings. This allows the prevailing failure mechanism to be dictated by corrosion on the joints, shown through Weibull plots demonstrating similar device characteristic life to that of the non-coated components. However, despite full coverage with conformal coating against corrosion, a new failure mechanism is introduced which supersedes corrosion impacts. The fully coated samples show no evidence of corrosion but show degraded thermal cycling performance due to the coating induced compression stress. The coefficient of thermal expansion mismatch between the conformal coating and the WLCSP can negatively impact device thermal cycling performance. In this case, possible coefficient of thermal expansion to the Z-axis direction serves as a driving force, which amplifies applied strain on the interconnects leading to reduced interconnect characteristic life and initial failure cycle count. Potential resolution to this is offered in the form of edgebond adhesive application. A combination of edgebond with conformal coating provides the full benefits of corrosion resistance while improving device reliability.

ACKNOWLEDGEMENTS

This work is a research project supported by Zymet and Cisco Component Quality and Technology group.

REFERENCES

1. M. Abtew, G. Selvaduray, Mater. Sci. Eng. R 27, 95 (2000)

2. D. Frear, H. Morgan, and J.H.Lau, eds. The Mechanics of Solder Alloy Interconnects, (New York: Van Nostrand Reinhold, 1994)

3. H.G. Song, J.W. Morris Jr., F. Hua, JOM 56, 30 (2002)

4. Bo Liu, Tae-Kyu Lee, and Kuo-Chuan Liu, J. Electron. Mater. 40(10), 2111 (2011)

5. A.J.Hale and H.S.Fosteh, J.Soc.Chem.Ind. 9, 2371 (1915)

6. A.Jermstad and A.Gaule, J.Inst. Met. 13, 1370 (1919)

7. B.Y.Wu, Y.C.Chan, and M.O.Alam, J.Mater.Res. 21(1), 62 (2006)

8. D.Li, P.Conway, and C.Liu, Corrosion Sci. 50, 995 (2008)

9. J.Y.Jung, S.B.Lee, H.Y.Lee, Y.C.Joo, and Y.B.Park, J. Electron. Mater. 37(8), 1111 (2008)

10. Tae-Kyu Lee, Bo Liu, Bite Zhou, Thomas Bieler and Kuo-Chuan Liu, J. Electron. Mater. 40(9), 1895 (2011)

11. P.Zhao and M.Pecht, IEEE Trans. on Device and Mat. Rel. 5(2), 268 (2005)

12. K.Kokko, L.Frisk and P.Heino, Soldering and Surface mount technology 22(3), 42 (2010)

13. D.Chen and M.Osterman, Proceeding of the IEEE Accelerated stress testing and reliability conference, Pensacola Beach, FL, (2016)

14. C.Yin, S.Stoyanov,C.Bailey, and P.Stewart, IEEE Trans. on Component, Packaging and Manufacturing Technology 9(11), 2210 (2019)

15. M.Serebreni, R.Wilcoxon, D.Hillman, N.Blattau, and C.Hillman, Proceeding of the 33rd Thermal measurement, Modeling and Mahangement Symposium, San Jose, CA, 40(2017)

16. H.Qi, M.Osterman, and M.Pecht, IEEE Trans. on Electronic Packaging Manufacturing 32(1), 32(2009)

17. H-.M.Tong, L.Mok, K.Grebe, H.Yeh, K.Srivastava, and J.Coffin, IEEE Trans. on Components, Hybrids and manufacturing technology 16(5), 571(1993)

18. S.Han, M.Osterman, S.Meschter, and M. Pecht, J. Electron. Mater. 41(9), 2508 (2012)

19. B. Medgyes and G. Ripka, IEEE proceedings 30th International Spring Seminar on Electronics Technology (ISSE), Romania, May, 429 (2007)

20. S.Wright, N.Nowell, and D.Field, Microscopy and Microanalysis, 17(3), 316 (2011)

21. H.Wu, F.Song, J.Lo,T.Jiang, K.Newman, and R.Lee, Proceeding of 59th Electronic Components and Technology Conference, San Diego, CA, 125 (2009)

22. B. Toleno and J. Schneider, Proceedings of 28th Int. Electron. Manuf. Technol. Symp., San Jose, CA, 299 (2003)

23. K. Meyyappan, A. McAllister, M. Kochanowski, and I. Hsu, IEEE Transactions on Components and
Packaging Technologies, 31(3), 670 (2008)

24. S. Perng, T-.K. Lee, and C. Guirguis, Proceedings of SMTA International, Rosemont, IL, 375 (2013)

PERIODIC PULSE PLATING OF MID-ASPECT RATIO PRINTED CIRCUIT BOARDS FOR ENHANCED PRODUCTIVITY

Carmichael Gugliotti, Rich Bellemare, Andy Oh, Ron Blake
MacDermid Alpha Electronics Solutions
Waterbury, CT, USA

ABSTRACT

Pulse plating of copper has typically found use in the plating of very difficult, high aspect ratio printed circuit boards. Its ability to provide throwing power deep within through holes with aspect ratios as high as 30:1 is well established. This technology has long been thought of as a high technology, high cost, specialty process applicable only to high end products. This paper will discuss the advantages that pulse plating offers over conventional DC copper plating in high volume production applications for panels with aspect ratios of up to 12:1. These advantages are reduced plating time, increased throughput, and reduced plated copper thickness on the panel surface while meeting minimum in-hole copper thickness requirements.

Key words: Pulse Plating, Copper Plating, Mid-Aspect Ratio.

INTRODUCTION

Pulse plating of copper has typically found use in the plating of very difficult, high aspect ratio printed circuit boards. Its ability to provide throwing power deep within through holes with aspect ratios as high as 30:1 is well established. This technology has long been thought of as a high technology, high cost, specialty process applicable only to high end products [1]. With the continued miniaturization of electronic components and the increased functionality of electronic devices, even simple technology circuit boards have become thicker and more complex. This has pushed the capabilities of conventional DC copper systems to their limits causing bottlenecks in throughput due to the excessive plating times required for thicker boards while also limiting finer line capabilities due to over-plating of the surface with copper to meet minimum in-hole copper thickness requirements.

Research has continued to improve DC plating systems but has started to see smaller and smaller degrees of improvement in being able to plate copper evenly in the center of holes in the thicker boards as well as minimize surface copper. As DC plating reaches its limits and technology continues to advance, a need for an economically feasible plating system has become increasingly necessary. A potential market is developing for a mid-aspect ratio pulse plating bath that can perform better than the typical high throw DC copper baths without the high cost of a high-end pulse bath.

BACKGROUND

Originally, printed circuit board designs were simple. They were typically thin and had minimal detail work on the surface. Conventional DC copper baths could easily meet the plating requirements of these designs. Often panels plated with 70-80% efficiency were acceptable. As electronics technology has advanced, there have been significant changes to PCB architecture. These changes include densification of circuitry, higher functionality, and thicker panels allowing for more to be done in a smaller area [2]. A large part of this has been driven by technology changes in the mobile phone market leading to smaller and more advanced phones.

As advancements have occurred, chemical suppliers have continued to improve their DC plating systems to meet new plating requirements. New DC baths have provided significant improvements to throwing power and thickness distribution. Many high-volume board designs however have advanced beyond the capabilities of DC plating technology due to the inability to meet throwing power requirements, leading to an over-plated surface, long plating time, and a significant waste of copper. The over-plated surface must be etched, increasing processing time and wasting copper. The over-plated surface also limits HDI (high density interconnects) designs due to lateral undercutting of the lines resulting in poor quality traces.

Pulse plating technology offers a substantial increase in performance over DC plating. Pulse plating is able to plate copper into deeper through holes and maintain an even plating thickness throughout the hole. It is also able to minimize surface copper by plating at a higher efficiency in the hole which results in savings both on anode costs and on etching. Pulse plating can maintain a 1:1 plating thickness ratio between the hole and surface allowing for a more precise thickness control and can operate at higher current densities. Current densities can be run higher than 30ASF and still give good results. The reduced surface copper makes it easier to final copper etch and more compatible with HDI designs.

Pulse plating technology has been used in plating copper for printed circuit boards for decades. The main drawback of pulse plating has been the high costs of the pulse rectifiers and the chemical additives. While pulse plating systems have typically been used for high aspect ratio circuit boards with difficult designs, they can also be modified to meet the requirements within the mid-aspect ratio segment. With the availability of lower cost pulse rectifiers,

pulse plating systems can be designed to provide the good throwing power and high throughput at economical operating costs that are specifically required for the mid-aspect ratio market segment. Currently, a 600amp DC rectifier might cost approximately $7,000 US while a typical pulse rectifier of the same capacity might cost approximately $13,000 US.

Figure 1. DC vs Pulse Rectifiers

This new pulse system must meet the performance requirements of high volume, mid-aspect ratio, HDI designs. The key factors to a successful system would be to maintain good throwing power, high throughput, minimal copper over plate, less copper etching, HDI capability, and simple pulse waveforms.

DC PLATING

Conventional DC or direct current acid copper plating is a well-established process entailing the use of cathodic current supplied by a DC rectifier to deposit a copper layer with good physical properties onto a circuit board from a plating solution containing copper sulfate, sulfuric acid, chloride ions, and a variety of additives that control the deposition process. These additives typically include a wetter, brightener, and a leveler.

Wetter

The wetter, typically a high molecular weight polyglycol, acts as a plating suppressor. When a direct current is applied, the wetter, in conjunction with the chloride, forms a semi-insulating blanket over the PCB surface which inhibits the migration of copper ions to the surface and controls the reduction of copper ions at the surface. This controlled initiation and grain growth of the copper deposit results in a smoother, more even coating.

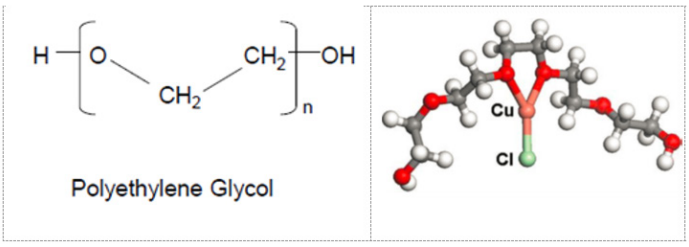

Figure 2. Sample Wetter Molecule

Brightener

The brightener, typically a low molecular weight sulfur compound, acts as an accelerator by forming low activation energy bridges to the copper surface. The brightener tends to increase the rate of formation of nucleation sites for copper grain growth and speed up the deposition rate. The result is a finer grained deposit with greater brightness.

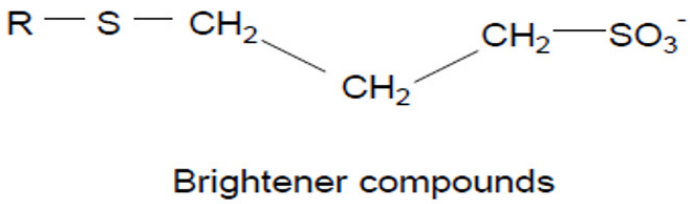

Figure 3. Sample Brightener Molecule

Leveler

The leveler acts as a secondary plating suppressor that slows the deposition rate on peaks at a microscopic scale to provide a further leveling of the deposit to produce a mirror like finish.

When current is applied in DC plating, an equilibrium is established in terms of additive adsorption, current density distribution, and plating rate. Though the additives, acting as deposition modifiers, redistribute current to a certain extent, the overall deposition is still governed by Faraday's Law. Outside surfaces and edges will accumulate higher charge densities and plate thicker than lower charge density areas such as internal recesses and internal hole walls of through holes.

Drawbacks of DC Plating

DC copper plating is limited by the efficiency at which it can plate into the hole as well as the evenness of the plating along the through hole walls. To compensate for this, PCB manufacturers have to over-plate the surface to meet the requirements inside the hole. The over-plated surface requires a greater amount of etching which increases time and cost in the process. Additionally, plating the extra copper requires more time thus reducing throughput along with the wasted cost of additional copper.

PULSE PLATING

In pulse plating, the solutions still contain typical components such as copper sulfate, sulfuric acid, chloride ions, and additives, but special rectification is used to vary the current using pulse waves throughout the plating cycle to disrupt the equilibrium formation of the additive films and redistribute current into low charge density areas. These pulse waves consist of a cathodic, or forward cycle, followed by a short, high current density anodic, or reverse cycle.

During the forward cycle, formation of the additive films and low energy bridges begins to occur as with DC plating. The high energy reverse pulse, which is distributed mainly around high charge density areas, then breaks the low energy brightener bridges in these areas while maintaining them in the low charge density areas (See Figure 4). With the next forward cycle, plating begins again

in a non-equilibrium state which the system tries to re-form but is unable to maintain due to the following reverse cycle. The effect of this is that a relatively high plating rate is maintained within the low charge density areas such as inside the through holes as the brightener bridges are maintained, while greater suppression is kept in the higher charge density areas due to the breakage of these accelerating bridges.

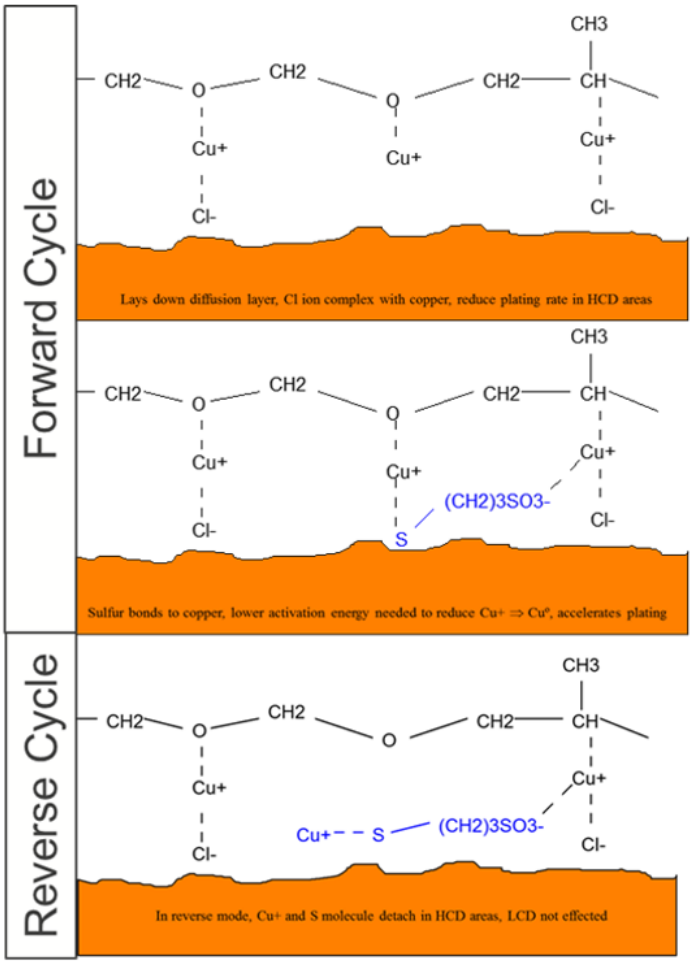

Figure 4. Pulse Cycle

There are a wide variety of pulse waves that can be used to modify current distribution and increase throwing power on a panel. These are typically expressed in terms of the ratio of forward to reverse time in milliseconds and forward to reverse current density in amps per square foot. Typical forward: reverse times are 100:5ms or 20:1ms with reverse currents of 1x, 2x, or 3x the forward current. The higher the negative current, the more aggressive the pulse cycle and the more matte the surface will appear. A multi-step process can be used to slowly reduce the reverse current as plating continues to give a more even, shiny appearance on the finished board without sacrificing throwing power.

Pulse Waves

Pulse waves can be designed in a variety of ways. A simple periodic pulse wave introduces a gap where there is no flow of current to the bath before returning to the forward current. The introduction of a reverse current is considered a periodic pulse reverse (PPR) and can include a dead time with no current or just switch between forward and reverse current. For this experiment, simple PPR waves were used. It is possible to create complex pulse waves by changing factors such as the reverse current, the pulse time, or the base current of the wave. Complex waves are not required for mid-aspect circuit board designs but are outlined in Figure 5.

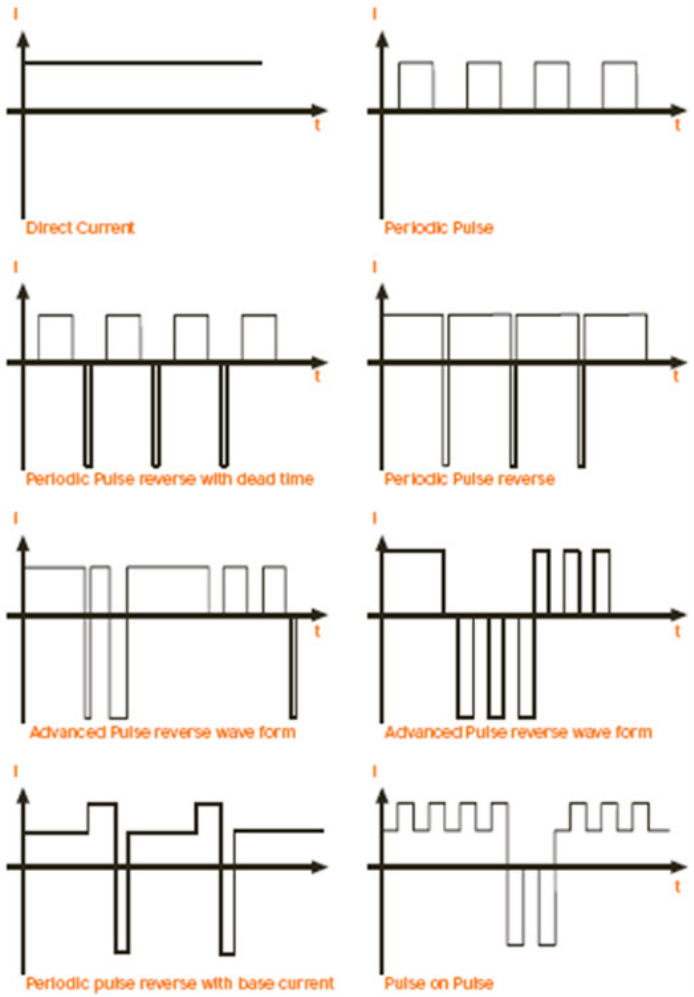

Figure 5. DC vs Pulse Cycles

EXPERIMENTAL

Experiment

A comprehensive DOE was done to compare the differences in performance between DC plating and three pulse cycles in a system designed for mid-aspect ratio panels. Panels were evaluated for appearance, throwing power in the hole and at the knee, and reliability. The panels used were two thicknesses, 1.6mm and 2.4mm thick, with a variety of hole sizes to provide a variety of aspect ratios for evaluation (see Table 1).

Table 1. DOE Conditions
***Percentages indicate the percentage of the plating cycle time**

Cycle	F/R Time Ratio (ms)	R/F Current Ratio	Forward Current Density (ASF)
DC	N/A	N/A	30
Single Step (Lower Frequency)	100/5	2X	30
Single Step (Higher Frequency)	20/1	2.5X	30
Multistep	20/1	3X-2X-1X 60%-20%-20%*	30

The primary attribute in pulse plating is throwing power, or the amount of copper plated in the hole compared to the copper plated on the surface. To maximize accuracy, each throwing power result was calculated from four measurements on the surface and two measurements in the hole as in Figure 6.

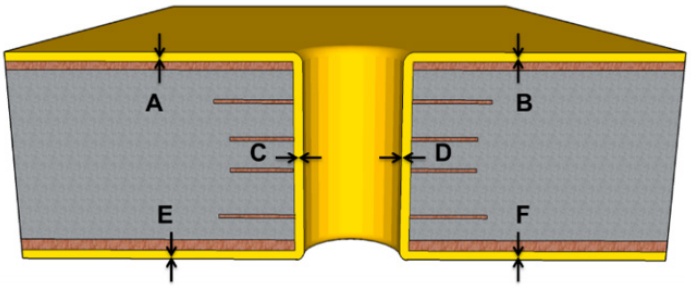

Figure 6. TP% Measurement Locations

The two measurements, C and D, in the hole were then averaged and divided by the average surface copper number, based on A, B, E and F measurements. The resulting number was then converted to a percentage for comparison for each test.

Throwing power was also evaluated at the knee of the hole. The throwing power at the knee was determined by taking the measurement at point B, from corner of the copper foil to the outside edge of the plated copper, and dividing by the thickness of the surface copper, A, multiplied by 100 (see Figure 7). Results were similar across all aspect ratios and panel thickness.

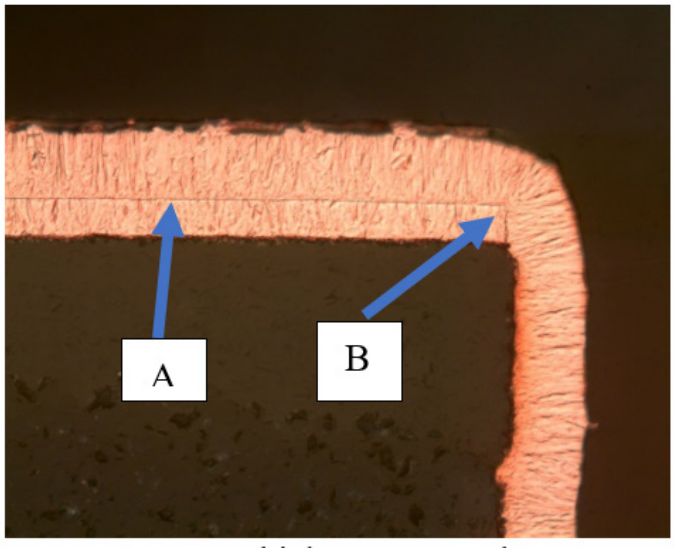

Figure 7. Knee thickness example

RESULTS

The results showed that pulse plating can be used to successfully plate boards of 1.6 to 2.4mm thick with aspect ratios of 12:1 or less, while easily maintaining 100% throwing power.

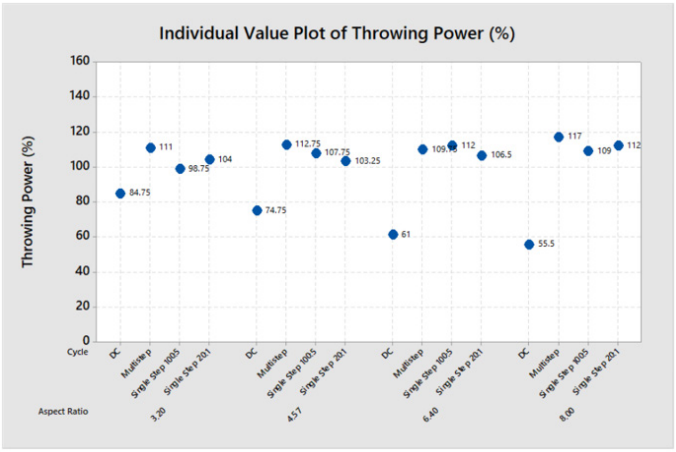

Figure 8. Throwing power on a 1.6mm board at 30ASF

In Figure 8, results compare a typical DC process to the mid-aspect ratio pulse bath with three different pulse cycles at various aspect ratios. Each set of data shows DC, a multistep process, single step 100:5, and single step 20:1. The aspect ratios were 1.2:1, 4.5:1, 6.4:1, and 8:1. The results show the ease of maintaining 100% throwing power for the three pulse plated sets compared to the DC plated set which dropped considerably as the aspect ratio increased. The DC plating began at 85% for the lowest aspect ratio hole and dropped to 56% for the highest aspect ratio hole.

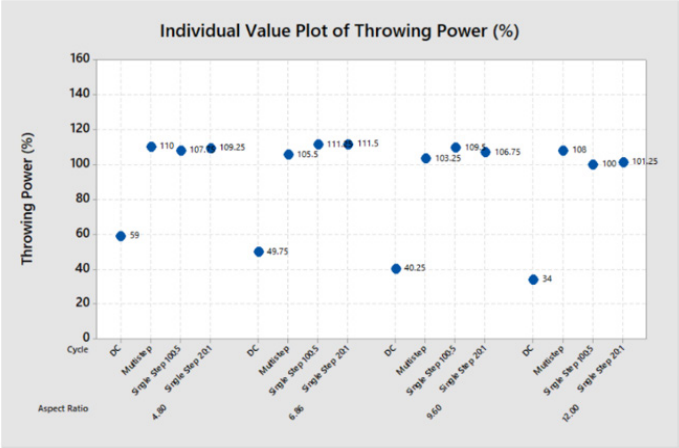

Figure 9. Throwing power on a 2.4mm board at 30ASF

Figure 9 shows similar results to Figure 8 with a 2.4mm thick panel. The 2.4mm panel had higher aspect ratios of 4.8:1, 6:1, 9.6:1 and 12:1. In this case, the trend was clearer with the mid-aspect ratio pulse bath easily maintaining 100% or greater throwing power while the DC bath started significantly lower at 59% and decreased to 34% at the higher aspect ratios.

Comparing the DC plating to the three pulse waves, there was no statistically significant difference in knee thickness with all cycles showing a knee thickness of 80-90% of the surface copper. It is important for the reliability of the through hole to have enough thickness of copper in this area. Thin knees can lead to cracking under thermal stress. A comparison of pulse plating vs. DC plating on mid-aspect ratio plated through holes can be seen in Figure 10.

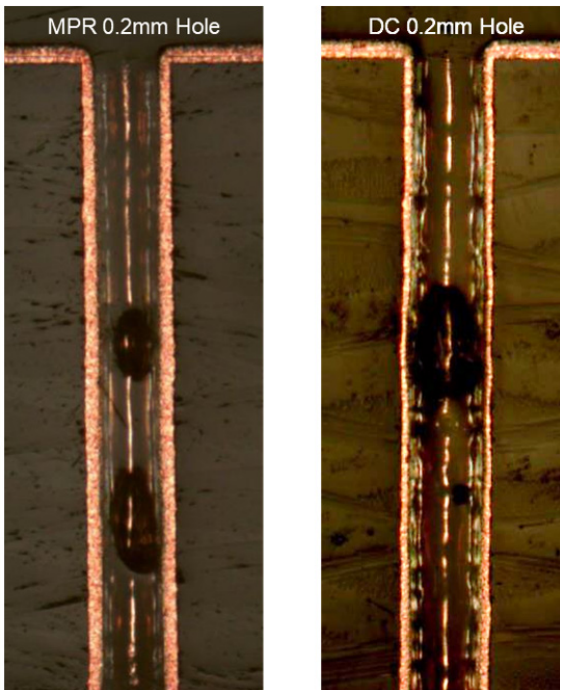

Figure 10. DC vs Pulse Plating on 0.2mm hole

The main effects were evaluated for throwing power on the 1.6mm and 2.4mm thick panels (Figures 11 and 12). The largest effect on throwing power was the cycle used, with DC plating showing significantly lower performance than any of the pulse cycles. Bath age, from 25Ah/L to 175Ah/L, was not significant based on the results. In the 1.6mm panel the hole diameter and aspect ratio did not show a large effect across the aspect ratios tested. In thicker panels there is a trend where the larger the hole diameter, the better the performance and the lower the aspect ratio the better the performance. This was based on the large contribution of the DC plated panels in the DOE due to the poor performance as aspect ratio increased and hole diameter decreased. Removing the DC results, there was no significant effect for the aspect ratios or hole diameter on throwing power.

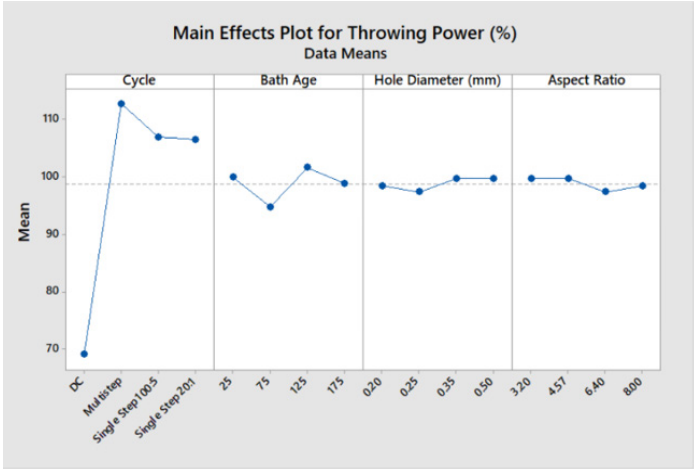

Figure 11. Minitab Main Effects Plot for 1.6mm Panels

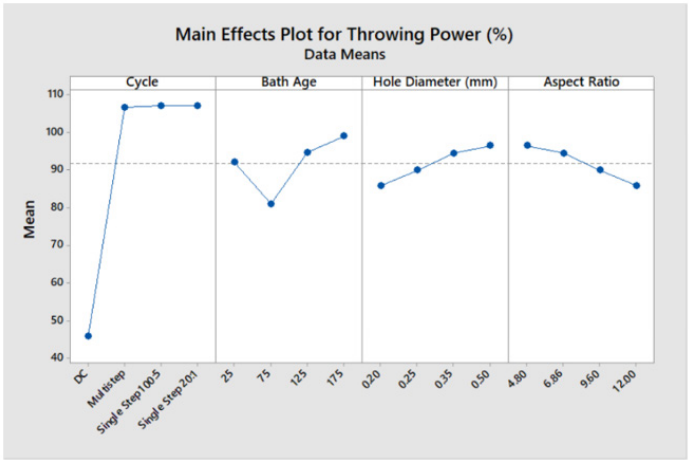

Figure 12. Minitab Main Effects Plot for 2.4mm Panels

The main effect for appearance was the cycle used. The DC plated panels showed the highest rated surface: mirror bright with no burning. The multi-step pulse cycle showed a slightly less shiny appearance. The single step pulse cycles tested showed a more

matte appearance with greater dullness in high current density areas. This is typical of pulse plated deposits. There were no significant interactions between the main conditions for both the 1.6mm and 2.4mm thick panels

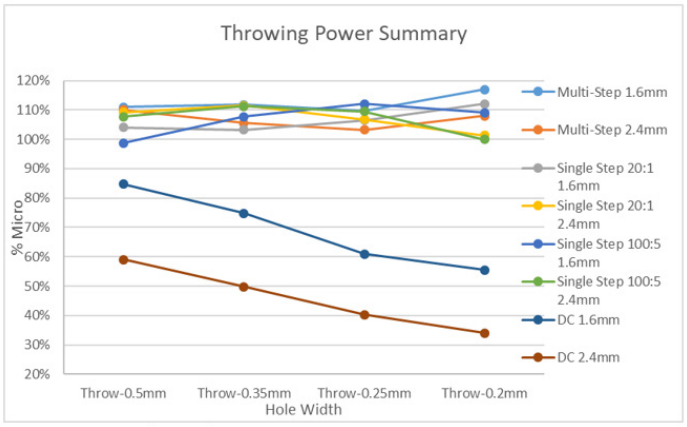

Figure 13. Throwing Power Summary

The throwing power summary graph (Figure 13) shows a comparison between all the cycles at each of the 4-hole sizes for 1.6mm and 2.4mm panels. The DC results were much poorer than the mid-aspect ratio pulse results. The two DC results showed a rapid deterioration in throwing power as the hole gets smaller and the aspect ratio increases. The pulse results were consistent across all the pulse waves and hole sizes, easily meeting the desired 100% throwing power requirement.

Reliability- Solder Shock

Panels plated in the standard DC bath and pulse bath were checked for reliability with multiple tests, including a six-time solder shock at 288°C for 10 seconds, five-time simulated IR reflow, and tensile and elongation testing. Solder shock results showed no cracks or severe hole wall pull away for any of the cycles tested.

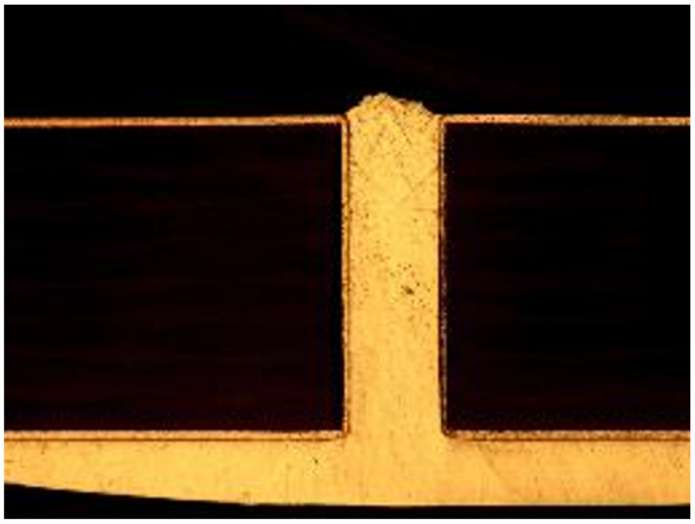

Figure 14. 6x Solder Shock at 50x magnification

Figure 15. 6x Solder Shock at 200x magnification

The two images above (Figures 14 and 15) show typical examples of solder shocked panels. There was no difference between the DC plated and pulse plated coupons. All coupons were checked at three and six times. Each coupon was laid flat atop solder at 288°C for 10 seconds per exposure time. Between exposures, the coupons were cooled down and then dipped in flux.

Reliability- Tensile and Elongation

For each DC and pulse cycle tested, a stainless-steel panel was plated with 3 mils (75µm) of copper as the bath aged. The panels were plated at 25Ah/L, 75Ah/L, 125Ah/L, and 175Ah/L. After plating, each foil was cut into 10 strips of 5" by ½" and baked at 125°C for 4 hours. After baking the samples were cooled and weighed. All testing for tensile and elongation were done on an Instron pull tester.

At each bath age, the four plating cycles were compared. The tensile strength remained over 30,000 PSI at all test points with a maximum of 45,000 PSI. The DC plating and multi-step cycles were slightly higher that the single step cycles (Figure 16).

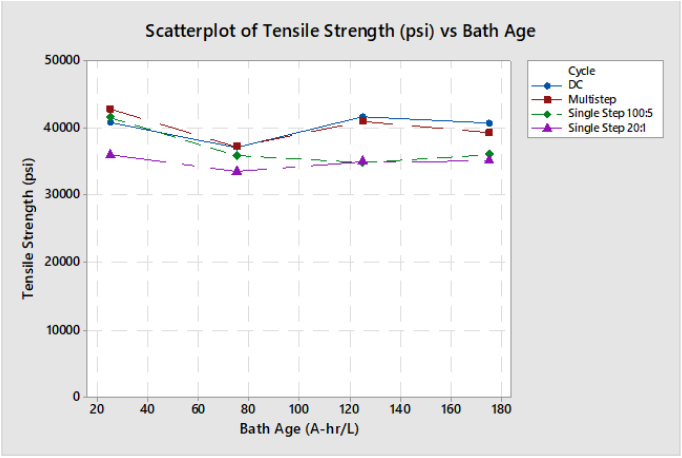

Figure 16. Tensile strength of various cycles compared to bath age

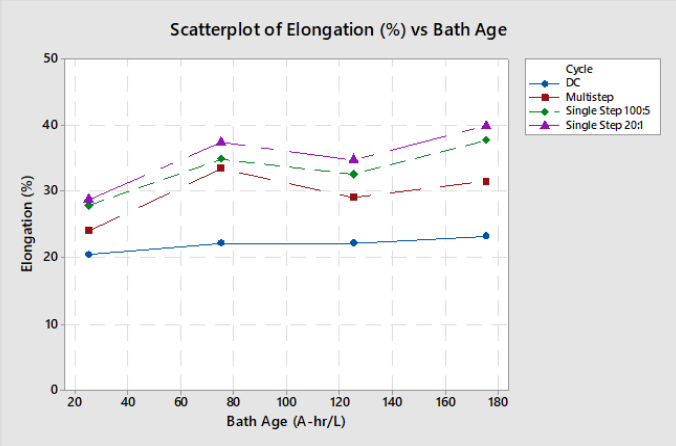

Figure 17. Elongation of various cycles compared to bath age

Elongation was also checked at each age point and showed results of 20% or greater. The elongation of pulse plated copper was consistently 10-20% greater than DC plating. The elongation climbed slightly as the bath aged and the single step 20:1ms pulse was always the highest.

Reliability- Reflow

Figure 18. Simulated IR Reflow Cycle

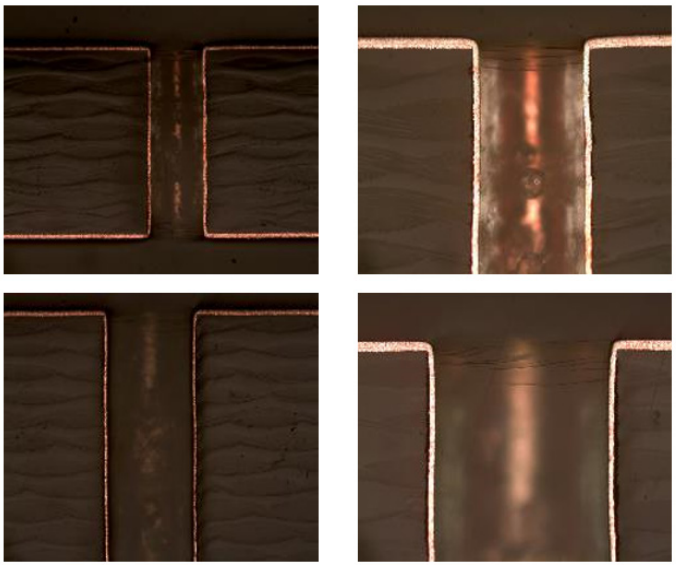

Figure 19. Cross Section photos of 5x IR reflow simulation

Panels were plated at various bath ages from 5Ah/L to 200Ah/L and cross sectioned to evaluate holes and microvias for separations and cracks after reflow simulation. There were no severe cracks or separations found with any of the cycles tested.

DISCUSSION

Consistency

Pulse plating offers a significant advantage over DC plating due to its ability to throw deep within a through hole while easily maintaining a 1:1 ratio of copper thickness within the hole and on the surface. This technique has potential use in high volume mid-aspect ratio applications where meeting the minimum thickness requirements within a hole without over plating the surface can result in significant copper savings and improved throughput. The savings obtained by these improvements can easily offset the higher cost of a pulse rectifier.

Cost Savings

As an example, assuming the values outlined in Table 2, a DC bath with 70% throwing power will need to plate an additional 10.9um of copper on the surface to meet the minimum 25.4um thickness requirements in the hole.

Table 2. Cost Saving Assumptions and Calculation

DC Bath	70%	Panels/day	1000
PPR	100%	Plating days/yr	250
Exposed Area	50%	Copper anodes	$3.00/lb
Wt of Cu/um/panel (18x24)	4.97g	A-min/25.4um	1200

Throwing Power (%)	Hole Wall Thickness (um)	Required Surface Cu (um)	Additional Cu (um)	Additional Cu Anodes	Savings (USD)
100%	25.4	25.4	10.9	6772kg (14,898lbs)	$44,692
70%		36.3			

This translates to a savings of approximately 15,000lbs of copper anodes per year in addition to the cost of not having to strip that amount of copper and treat the generated waste.

In addition to the savings in copper usage and treatment, there is also a throughput increase. Under the assumptions above in Table 2, the additional copper plated to meet the thickness requirement in the hole requires 17 minutes of additional plating time over the 40 minutes required to plate at 100% throwing power. This represents an additional 11 loads per day, or a potential increase in throughput of approximately 43%.

Table 3. Increased Throughput Calculation

Bath	TP (%)	Cu Thick in Hole (um)	Surface Cu Required (um)	Cycle Time @30ASF (min)	Loads per Day (24hr)
DC	70	25.4	36.3	57.1	25.2
PPR	100		25.4	40	36
Increased Throughput			**42.9%**		

CONCLUSION

As electronics continue to evolve, and board architecture changes to accommodate new designs, the use of pulse plating for mid-aspect ratio PCBs to maintain production throughput can be a viable option to conventional high throw DC plating.

Pulse plating can plate a copper deposit with excellent physical properties deep into a through hole with 100% throwing power at relatively high current densities, allowing a fabricator to maintain high throughput, minimize copper usage, and reduce etching and waste treatment volumes. Though rectifier costs are still higher for pulse plating than DC plating, costs have come down significantly and can be further offset due to the process savings of pulse plating. Considering the drawbacks of DC plating in terms of speed and thickness distribution, pulse plating can be a viable economical solution for high volume plating of thicker mid-aspect ratio products.

ACKNOWLEDGEMENTS

The authors would like to thank the various technical centers from MacDermid Alpha Electronic Solutions that did some of the testing and data collection. In addition, a special thank you to George Viola and American Plating Power for providing quotes and additional information about pulse and DC rectifiers.

REFERENCES

[1] N. Osero, "An Overview of Pulse Plating", Plating and Surface Finishing March 1986 pp. 20-22

[2] R. Bellemare, C. Gugliotti, "The Effect of Board Design on Electroplated Copper Filled Thermal Vias For Heat Management", Proceedings of SMTA International March 2017

[3] M. Nikolova, J. Watkowski, "Innovative High Throw Copper Electroplating Process for Metallization Of PCB", Proceedings of Pan Pacific Symposium January 2011

BIOGRAPHIES

Carmichael Gugliotti is a Metallization Applications Manager at MacDermid Alpha Electronic Solutions based in Waterbury, CT. He holds a Bachelor's of Science in Chemistry from the University of Connecticut. He has worked on new metallization technologies for acid copper plating with a focus on via fill, high throw DC copper, and pulse plating.

EDGEBOND AND EDGEFILL INDUCED LOADING EFFECT ON LARGE WLCSP THERMAL CYCLING PERFORMANCE

[1]Andy Hsiao, [1]Greg Baty, [2]Edward Ibe, [2]Karl Loh, [3]Steven Perng, [3]Weidong Xie, and [1]Tae-Kyu Lee
[1]Portland State University, Portland, OR
[2]Zymet, East Hanover, NJ
[3]Cisco Systems, San Jose, CA

ABSTRACT

Various external load conditions affecting components on electronic devices and modules are constant factors, which need to be considered for the component long-term reliability. Recently, to enhance the high stress component thermo-mechanical cycling performance, various types and configuration using edgebond and edgefill technology are introduced and tested. These applications induce a multi-axis loading condition, which alter the degradation mechanism and failure location during thermal cycling, which need closer investigation. In this study, high stress 12x12mm^2 wafer level chip scale packages (WLCSP) were selected and subject to thermal cycling with full-edgebond, dot-edgebond and edgefill adhesive, which improves the characteristic lifecycle numbers base on the configurations, but altered the failure location due to different stress conditions. The -40 to 125°C thermal cycling profile revealed localized degradation per configuration during thermal cycling, showed a shift of the crack propagation path, based on full-edgebond, dot-edgebond and edgefill adhesive sample conditions. Through these series of observation, the interconnect thermal cycling degradation mechanisms are able to be explained. The correlation between the stress condition and microstructure are presented and discussed based on Electron backscattered diffraction (EBSD) analysis.

INTRODUCTION

It is well known that wafer level chip scale packages (WLCSP) are presenting shorter characteristic lifecycle numbers subject to thermal cycling due to the higher coefficient of thermal expansion (CTE) mismatch with the PCB. [1-3] But the industry sector on Internet Of Things (IoT) and industry automation are in high speed in transformation where WLCSP are playing a crucial role due to its form factor and simple structure, which obviously brings an economical benefit. But at the same time it is important to enhance the lifecycle time for these WLCSP for higher reliability since the automation and controllability is crucial to the safety of the electronic system. With higher function per component need, increasing in WLCSP body size is a constant challenge, since larger WLCSP have higher thermal coefficient mismatch resulting in a higher stress at the corner interconnects between the component and PCB. [4,5] As shown in Figure 1, larger WLCSP body size components show significantly lower thermal cycling performance.

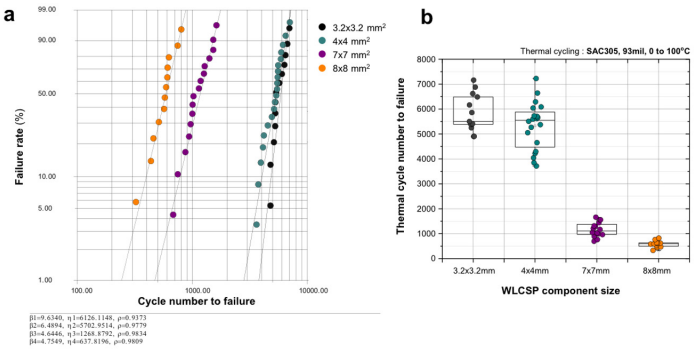

Figure 1. Various body size WLCSP thermal cycling performance (a) Weibull distribution and (b) Failure cycle distribution per WLCSP size. All WLCSP size components with 0 to 100°C thermal cycling profile with 93mil PCB thickness.

The selected components in Figure 1, were tested at the same testing thermal cycling condition, 0°C to 100°C with a 10min dwell time on 2.4mm (93mil) thickness PCB and components were all with SAC305 solder balls and 0.4mm pitch configuration. As shown in the figure, having a WLCSP larger than 8x8mm^2 in body size will have a high chance to demonstrate a thermal cycling performance less than ~300 cycles, which will be a limitation factor for WLCSP for long-term reliability application. Overcoming this challenge and improving the thermal cycling performance of WLCSP can be achieved by a few approaches. One of them is the strengthening of the solder joint material itself by applying a new solder alloy composition. But this also has a limitation since strengthening the solder joint can pose higher stress at the interface layer resulting in a crack free solder joint but a damaged dielectric layer at the package interface. Another approach is the enhancement of the total package or module, so that the stress per solder joint is reduced to a lower level, which is the use of underfill material. But even if it is a mature technology, the underfill process at the BGA board level component has a few challenges associated with no-clean flux residue, which can negatively impact the interface between the underfill material and the board interface, especially with smaller pitch and larger WLCSP body size components. The re-workability of large underfilled components is also a factor, which needs to be thoroughly considered. Larger WLCSP components with fully

underfilled configuration will be more difficult to be removed and re-worked. An alternative approach is a more localized enhancement using edgebond materials with less volume adhesive. Since the outer array solder joints in WLCSP experience most of the damage accumulation during thermal cycling, an enhancement targeting those solder joints can result in a higher reliability and long-term thermal cycling performance.[6] But unlike smaller WLCSP with edgebond adhesive, the larger WLCSP are expected to behave different during thermal cycling with more thermo-mechanical fluctuation of the silicon die due to warpage. Implementing the edgebond on WLCSP components is expected to alter the shear fatigue mode and degradation mechanism due to the restriction of the corner joint location strain, which is usually caused by large CTE mismatch. To enable a more detailed and in-depth analysis, the grain structure development inside the solder joints were observed and signature microstructures are identified to understand the behavior of the interconnects on edgebond applied and thermal cycled components.

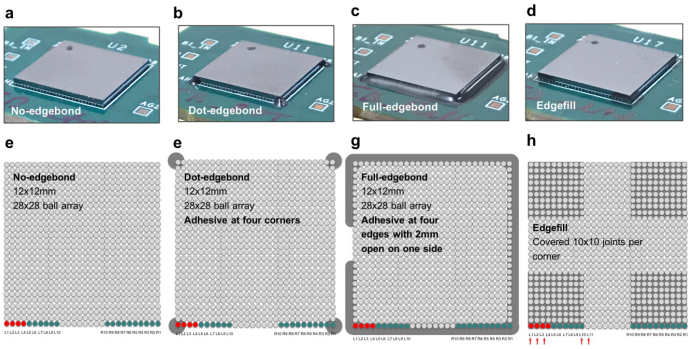

Figure 2. Edgebond sample component picture (a-d) and top view schematic configuration and ball array (e-h). (a) No edgebond configuration, (b) Dot edgebond, (c) Full Edgebond, and (d) Edgefill configuration.

EXPERIMENTAL PROCEDURE

Body size of 12x12x0.725 mm^3 with 0.4mm pitch, 250µm solder ball diameter WLCSP components were used in this study. Solder balls attached to the packages were all composed of Sn-4.0Ag-0.5Cu(wt%)(SAC405). The parts were board-assembled on 1.6mm (62mil) high glass transition temperature (T_g), FR4-printed circuit boards with OSP surface finishes with a thermal profile of peak temperatures of 240°C, 60 seconds above the liquidus temperature. All components were assembled with SAC305 solder paste. For edgebond process, commercially available reworkable edgebond adhesive was selected. A high T_g 134°C and low CTE 30ppm/°C reworkable edge-bond material was processed. The edgefill material has a slightly different T_g of 119°C but same low CTE of 30ppm/°C. The edgefill adhesive material was only available with a relatively lower T_g compared to the edgebond material, which potentially have an impact on the thermal cycling performance. The adhesive was applied to the WLCSP in three different configurations ; Dot-edgebond, Full-edgebond and Edgefill. As shown in Figure 2(b,f), the Dot-edgebond is a configuration, which has the four corner regions with minimal adhesive applied. The penetration of the adhesive was minimal and only covered one solder joint at the corner. The Full-edgebond configuration is a configuration, which has all four edges with adhesive applied with a small opening of 2mm in one of the edge regions. The penetration of the adhesive was also minimal and did not progress to the second row inside the component. Figure 2(d,h) presents the edgefill configuration, a partial underfill configuration, which penetrated into the four corner region and covered 10x10 solder joints per corner. Figure 2(a)-(d) shows the actual picture of each configuration and Figure 2(e)-(h) shows the schematic top view and adhesive penetration per configuration. To prevent voiding due to moisture releasing from PCB material in curing cycle, test boards are pre-baked for 4 hours at 125°C after the adhesive was applied. The edgebond adhesives were dispensed at room temperature using a pneumatic, hand-held dispenser. The board was then cured at 150°C for 30 minutes. For thermal cycling, samples were cycled from -40 to 125 °C at a ramp rate of 10°C per minute with 10 minutes of dwell time. A continuous resistivity measurement using a datalogger was applied for each channel in-situ monitoring during the test. The failure criterion in this study was based on the JESD22-A104D standard [7], a 20% increase of the peak resistivity for continuous five cycles relative to the initial value. The thermal cycling results for each condition were plotted as Weibull distribution plots. Cross-sectional analysis using optical microscope with bright light and polarized light and electron backscattered diffraction (EBSD) imaging were applied to observe the evolution of the microstructures and the locations of the solder joint cracks.

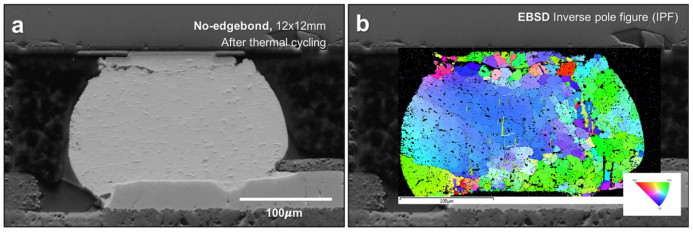

Figure 3. (a) SEM of 12x12mm² WLCSP package corner after thermal cycling to failure. (b) associated electron backscattered diffraction (EBSD) inverse pole figure image.

RESULTS AND DISCUSSION

As shown in Figure 3, thermal cycling induce a degradation in the microstructure indicated as a grain refinement and grain recrystallization. Figure 3(a) shows the crack in a solder joint in the 12x12mm^2 WLCSP package corner after thermal cycling, in this case a selected joint after 400 cycles to failure. The associated electron backscattered diffraction (EBSD) inverse pole figure image in Figure 3(b) reveals the fine grain structure near the crack propagation path. This development structure is well explained with the development of sub-grain boundaries with low angle boundary evolution during thermal cycling, which is shown in Figure 4. [8,9]

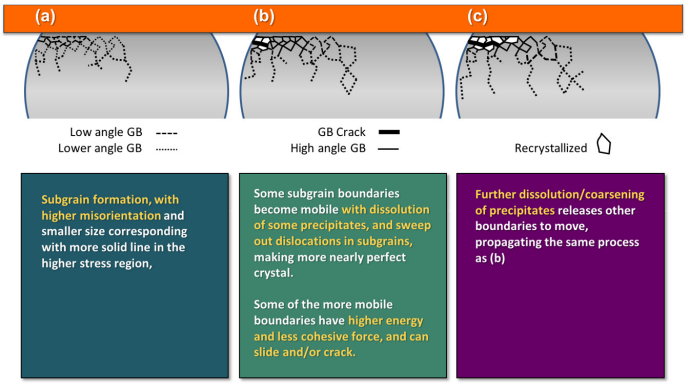

Figure 4. Crack initiation and propagation mechanism in solder joints during thermal cycling.[8]

In earlier study, a series of 12x12mm² WLCSP were thermal cycled to 100, 200, 300 and 400 thermal cycling numbers and are subject to cross section to observe development of grain refinement, recrystallization and their correlation to the crack propagation.[10] Figure 5 shows the distribution of fine grained structure and the crack propagation path per solder joints, for five solder joints from each corner. TC0 indicates the initial state and TC400 indicates 400 thermal cycles.

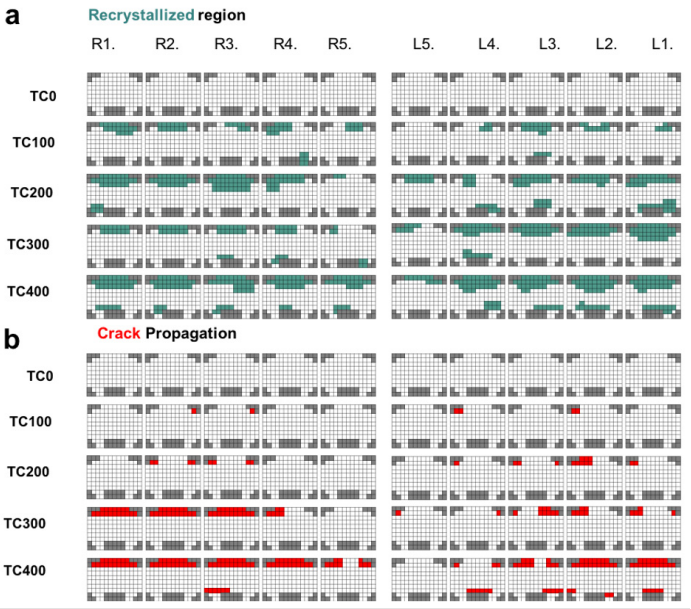

Figure 5. 12x12mm² WLCSP after segmented thermal cycling. (a) Recrystallization region and (b) Crack initiation and propagation path per solder joints after thermal cycling.

Beginning from the initial state cross section, an evolution of fine grain structure can be observed from the corner solder joints developing further into the inner solder joints once the cycle number reached 100. (Figure 5(a)) The associated crack location indicated per joints are shown in Figure 5(b). The crack developed also from the corner location solder joints at the package side interface then penetrated further with higher thermal cycling numbers to the inner solder joints. Given the fact that the damage accumulation with grain refinement and crack initiation are mostly from the corner solder joints, based on this observation an enhancement focusing on the corner location seems to be an effective approach.

Thus, three different edgebond configurations were selected and applied. As already shown in Figure 2(b,f), the dot-edgebond configuration targeted the corner joints to be secured, compared to the full-edgebond configuration, which covered the four full edges but not penetrated into the component to ease the rework process. Having the adhesive only at the edge of the component also mitigated the interaction between the residual flux and the adhesive and did not cause any weak bonding at the PCB to adhesive interface. The weak interface between the residual flux and the adhesive is often a reason for a degraded thermal cycling performance, thus an adhesive avoiding the region where flux resides have a higher chance to avoid the complication. The thermal cycling results in a Weibull plot for the dot and full-edgebond configurations are presented in Figure 6(a), which are also compared to the baseline of no-edgebond applied samples. The components without any enhancement methods applied, showed a characteristic cycle number of around 311 cycles. As indicated in Figure 6(b), the no-edgebond applied components all failed around 300 cycles with a narrow data spread. But with edgebond applied, the characteristic life cycle number increased to 843 cycles and 3088 cycles, for dot-edgbeond and full-edgebond applied components, which is an increase of lifecycle time for 271% and 992% respectively.

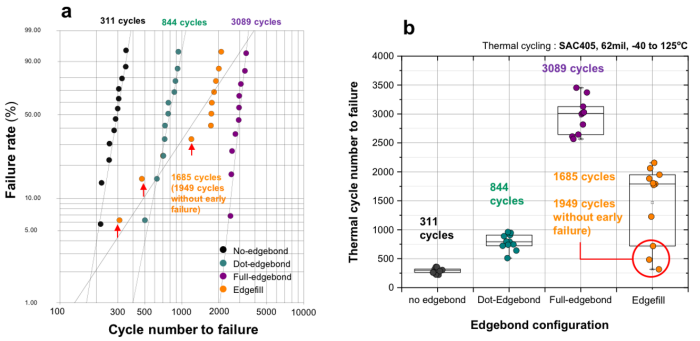

Figure 6. Thermal cycled WLCSP with no-edgebond, Dot-edgebond, full-edgebond and Edgefill configuration. (a) Weibull and (b) failure cycle distribution plot.

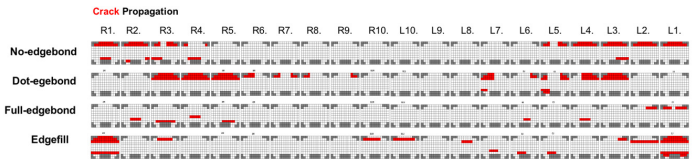

Figure 7. Thermal cycled WLCSP with no-edgebond, Dot-edgebond, full-edgebond and Cornerfill configuration. Crack propagation path indicated in red.

The main reason for this improvement in thermal cycling performance can be derived from the crack location map shown

in Figure 7. The outermost rows were cross sectioned to reveal the solder joints and ten joints from the right and left side corners are presented in Figure 7. The location of the solder cross section regions are indicated in Figure 2(e-h). The crack propagated regions are indicated in red. Compared to the no-edgebond component, the dot-edgebond cross section revealed the two solder joints from each corner are crack free with crack propagation in the third solder joints from the corners. All of the crack propagation path were located at the package side interface. Four solder joints from the right side corner (R1-R4) are presented in Figure 8(b).

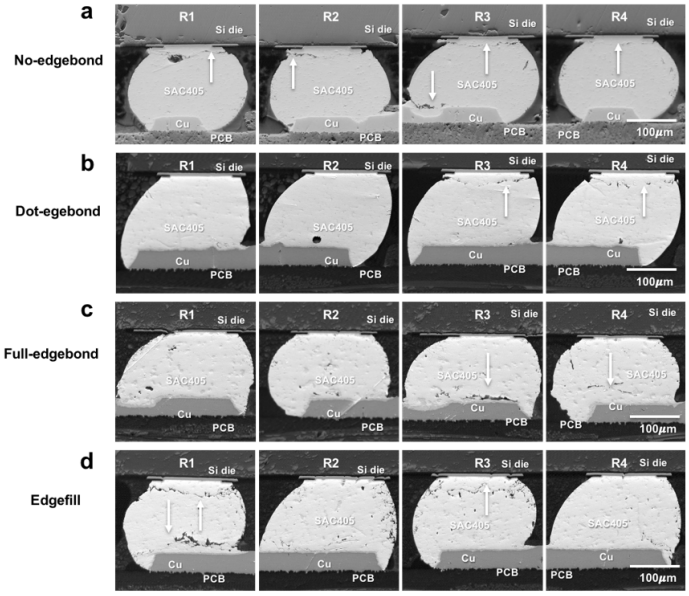

Figure 8. SEM images from R1 to R4 per edgebond configuration. (a) no-edgebond, (b) Dot-edgebond, (c) Full-edgebond and (d) Edgefill solder joints. Location indicated in Figure 2(e-h).

Crack location paths are indicated with the white arrows. Compared to the dot-edgebond sample, the full-edgebond components show a crack propagation path at the board side interface. Figure 8(c) show that the board side cracks are actually partial cracks inside the solder joint. Given the fact that these edge located solder joints, which are the outmost row solder joints, were covered with the adhesive, shear and tension of the solder joints are limited and show partial crack propagation instead of full cracks. The associated four solder joints from the right side corner (R1-R4) shown in Figure 8(c), which are indicated in Figure 2(g). Since the full-edgebond components were in the thermal cycling chamber for the longest among the three configurations, the Ag_3Sn intermetallic phase show the most accumulated size increase. The configuration which shows an intermediate improvement in thermal cycling performance was the edgefill configuration shown in Figure 2(d,h). Unlike the dot-edgebond and full-edgebond configuration, the edgefill adhesive penetrated the component and covered 10x10 solder joints per corner, where the 12x12mm^2 WLCSP has 28x28 solder ball array. The Weibull plot in Figure 6(a) for edgefill indicated characteristic lifecycle number of 1684 cycles or 540% improvement compared to the no edgebond applied WCSP. Three of the sample though show an early failure deviated from the general beta slope, which are indicated with red arrows, which indicates a possibility of two different failure modes. Considering these early failures as abnormal failure components and deriving the characteristic life cycles, the life cycle number increases to 1949 cycles. The crack propagation path were found at corner joints both at the package side and board side interface (Figure 8(d)) revealing a possibility of a localized degradation mechanism, on corner joints which are not fully covered with the Edgefill adhesive. The selected cross section in Figure 8(d) is the component, which failed at the 482 cycles. A crack propagation path at the board side interface is observed with additional crack path at the package side interface in R1 and R3. Since thermal cycling induces not only shear deformation but also tension and compression strain to the solder joints, it is valuable to see the WLCSP top surface Z-axis height variation between room temperature and elevated temperature.

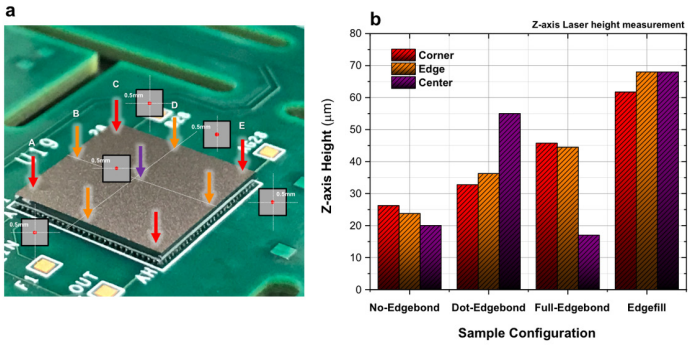

Figure 9. Linear Laser height difference measurement between room temperature and at 125°C Z-axis height. (a) Measurement location, Corner, edge and center, (b) Z-axis height difference per WLCSP configuration.

A linear laser measurement at corner, edge and center location per WLCSP with dot-edgebond, full edgebond, and edgefill configuration are compared to no edgebond applied WLCSP. The height difference between room temperature and at 125°C Z-axis height are shown in Figure 9. The measurement at corner locations are 0.5mm from two edges, edge location at 6mm from corner and 0.5mm from the WLCSP edge, and center location at 6mm from the two WLCSP edges as indicated in Figure 9(a). The no edgebond applied WLCSP show a lower difference in height, with dot-edgebond samples a higher height difference at the center location. Compared to the dot-edgebond, the full edgebond show less height difference at the center but an overall displacement at the corner and edge locations. But overall height difference was observed with edgefill WLCSP configuration. The main reason for a higher displacement range among all samples configuration, the lower T_g property for edgefill material can be the potential cause for the Z-axis expansion, which also contributed to a shorter characteristic life cycle performance compare to full edgebond configuration. To visualize the residual stress and lattice strain per solder joints per each configuration, an EBSD analysis was performed and the

resulted images are shown in Figure 10 for the dot-edgebond, Figure 11 for the full edgebond, and Figure 12 for the edgefill WLCSP after thermal cycling to failure.

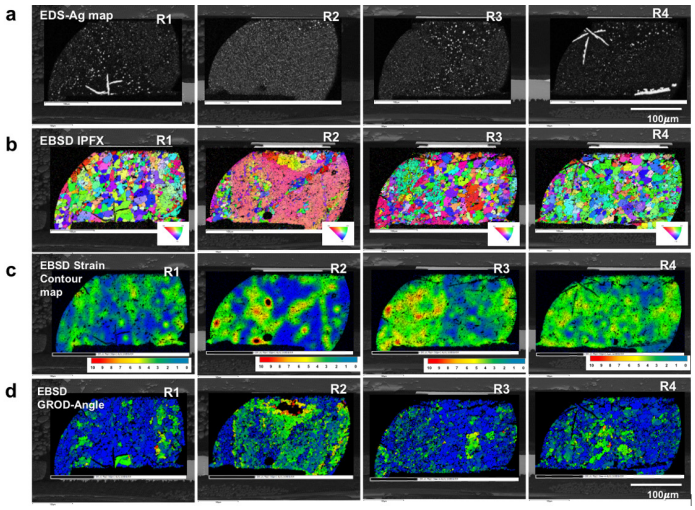

Figure 10. Dot-Edgebond WLCSP after thermal cycling to failure (R1, R2, R3, R4 in Figure 8(b)). (a) EDS-Ag map, (b) EBSD Inverse pole figure (IPF) image, (c) Strain contour map, and (d) EBSD Grain reference orientation deviation (GROD) map.

In Figure 10(a) the EDS Ag map indicates the Ag_3Sn intermetallic precipitates, which are often a good indicator where plastic deformation occurred in solder joints. The solders in Figure 10, R1 to R4 are the solder joints shown in Figure 8(b). R1 and R2 joints do not contain any solder crack since the dot-edgebond material at the corner region secured the two joints from degradation. The relative fine Ag_3Sn distribution in R1 and R2 also shows that the plastic deformation in these two joints are kept minimal. Compared to the R1 and R2, R3 and R4 show full propagated cracks near at the package side interface and the Ag_3Sn distribution map shows accumulation in the solder joints which are also associated with a grain refinement visible in the IPF map Figure 10(b) R3 joint. The associated strain contour maps reveal a well distributed high level strain, which can be compared to the low level of strain distribution in R1 joint which enhanced by the dot edgebond. The strain contour map is converted from scanned EBSD information based on local misorientation and can identify the localized grain region, which measures the level of deviation from the theoretical, non-strained lattice, revealing a distribution map of relatively higher plastic deformation regions. [11] The GROD map in comparison reveals indirectly the relative residual stress level compared to the adjacent grain, by revealing the level of tilting per individual grain compared to a grain orientation reference. [11]. Comparing the two EBSD scanning based information conversion, the relative level of strain and stress for each solder joint can be analyzed. For example, the residual stress level in R2 is higher than R3 in Figure 10(d), which indicates that R3 is already plastic deformed with low level of residual stress, but R2 residual stress is high since it is not yet plastic deformed.

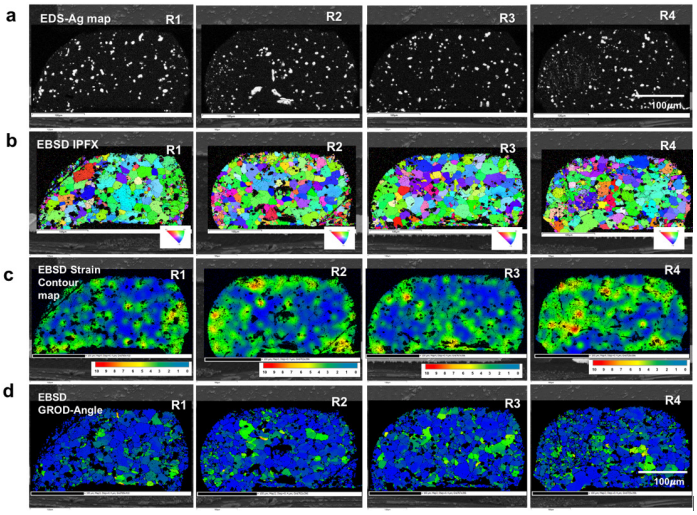

Figure 11. Full Edgebond WLCSP after thermal cycling to failure (R1, R2, R3, R4 in Figure 8(c)). (a) EDS-Ag map, (b) EBSD Inverse pole figure (IPF) image, (c) Strain contour map , and (d) EBSD Grain reference orientation deviation (GROD) map.

In Figure 11, the full edgebond applied WLCSP shows a larger in size Ag_3Sn IMC distribution since the components were in thermal cycling condition until 3089 cycles, with constant heat exposure. The associated Sn grain sizes are also larger in Figure 11(b) IPF map with relatively low level of strain and stress. (Figure 11(c) and (d))

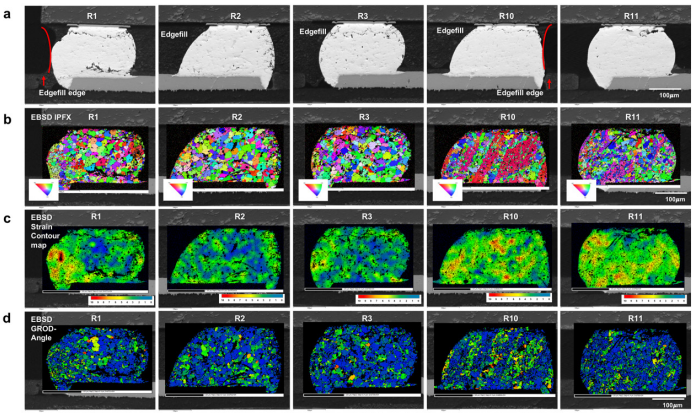

Figure 12. Edgefilled WLCSP after thermal cycling to failure (R1, R2, R3, R10 and R11). (a) SEM, (b) EBSD Inverse pole figure (IPF) image, (c) Strain contour map , and (d) EBSD Grain reference orientation deviation (GROD) map. Redlines in (a) indicated the edge of the edgefill region.

A mixed phenomenon can be observed in edgefill WLCSP shown in Figure 12. Solder joints R1-R3 (Figure 8d) and R10,R11 from the Edgefill component are presented. The location of the observed solder joints are indicated in red arrows in Figure 2(h). The inverse pole figure maps (Figure 12(b) and the strain contour maps (Figure 12(c)) indicated that the right side of R1 retains a higher stress region compared to R2 and R3 solder joints. R10 also shows a higher stress intensity distribution, which is a solder joint located at the edge of the edgefilled region. The outside edge of

the edgefill adhesive is indicated in red lines in Figure 12(a). R11 is the first solder joint outside the edgefill region, which contains a wider opened crack at the upper right shoulder region. Based on these EBSD results, it seems that the corner location solder joints inside the edgefill regions are in higher tension and residual stress, which is a direct indication of further fracture development, thus crack propagation. Compared to the R1 and R10, which are the solder joints which are at the end of the edgefill have significantly higher strain level compared to R2 and R3, which are inside the edgefill region. Knowing the relative strain level and stress level, the localized degradation status can be identified, which benefits the analysis, which helps to understand the degradation mechanism.

CONCLUSION

In this study, high stress 12x12mm^2 wafer level chip scale packages (WLCSP) were selected and subject to thermal cycling with full-edgebond, dot-edgebond and edgefill adhesive, which improves the characteristic lifecycle numbers base on the configurations, but altered the failure location per configuration. The -40 to 125°C thermal cycling revealed localized degradation per configuration during thermal cycling, showed a shift of the crack propagation path, based on full-edgebond, dot-edgebond and edgefill adhesive sample conditions. But with edgebond applied, the characteristic life cycle number increased to 843 cycles and 3088 cycles, for dot-edgbeond and full-edgebond applied components, which is an increase of lifecycle time for 271% and 992% respectively. With edgefill application, a characteristic lifecycle number of 1684 cycles or 540% improvement was observed. The edgebond adhesive provided a vast increase of thermal cycling performance with minimal coverage. The EBSD analysis on edgebond covered and non-covered joints indicated a stress intensity distribution, that enables the visualization of the solder joints and indicated the joints, which are in higher chance of crack initiation and propagation.

ACKNOWLEDGEMENTS

This work is a research collaboration project supported by Zymet and Cisco systems for their board assembly support.

REFERENCES

1. John H. Lau and S.-W. Ricky Lee, "Effects of Build-Up Printed Circuit Board Thickness on the Solder Joint Reliability of a Wafer Level Chip Scale Package (WLCSP)", IEEE Transactions on components and packaging technologies, 25(1), 3-14 (2002)

2. J.W.Yoon, J.H.Bang, Y.H.Ko, S.H.Yoo, J.K.Kim and C.W.Lee, "Power Module Packaging Technology with Extended Reliability for Electric Vehicle Applications", J. Microelectron. Packag. Soc., 21(4), 1-13 (2014).

3. Weidong Xie, Tae-Kyu Lee, Kuo-Chuan Liu, and Jie Xue, "Pb-free solder joint reliability of fine pitch chip-scale packages", IEEE 60th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, June (2010)

4. S. Terashima, T. Kohno, A. Mizusawa, K. Arai, O. Okada, T. Wakabayashi, M. Tanaka, K. Tatsumi, "Improvement of Thermal Fatigue Properties of Sn-Ag-Cu Lead-Free Solder Interconnects on Casio's Wafer-Level Packages Based on Morphology and Grain Boundary Character", Journal of Electronic Materials, 38(1), 33-38 (2009)

5. W.K. Choi and H.M. Lee, "Effect of soldering and aging time on interfacial microstructure and growth of intermetallic compounds between Sn-3.5Ag solder alloy and Cu substrate", Journal of Electronic Materials, 29(10), 1207-1213 (2000)

6. Andy Hsiao, Kola Akinade, Cherif Guirguis, Edward Ibe, Karl Loh and Tae-Kyu Lee, "The impact if conformal coating on WLCSP thermal cycle performance : Degradation mechanism and mitigation method", Proceedings of SMTA International, September 17-21, Rosemont, IL, 745-750 (2017)

7. JEDEC Standard, JESD22-A104D, Thermal cycling, March 2009, http://www.jedec.org/standards-documents

8. Tae-Kyu Lee, Thomas Bieler, Choong-un Kim et al., "Fundamental of solder and interconnect technology", Springer, Chapter 5, 132-133 (2014)

9. S. Park, R. Dhakal, L. Lehman, and E. Cotts, "Measurement of deformations in SnAgCu solder interconnects under in situ thermal loading", Acta Mater., 55(9), 3253-3260 (2007)

10. Andy Hsiao, Mohamed Sheikh, Tony Crespo and Tae-Kyu Lee, "Compression and tension stress effect on WLCSP thermal cycling performance", TMS2019, San Antonio, TX, March 11 (2019)

11. S.Wright, N.Nowell, and D.Field, "A Review of Strain Analysis Using Electron Backscatter Diffraction", Microscopy and Microanalysis, 17(3), 316 (2011)

Welcome New SMTA Members!

Cesar Alberto
NEOtech

Lavanya Ashok Swaminathan

Tadeh Avanessian
Keysight Technologies

Alexander Baer

Nupur Bajad
Analog Devices, Inc

Emily Belfield
Indium Corporation

Jan Besser
Merck Performance Materials

David Bowersock
Ducommun Incorporated

Amanda Brewer
Veris Mfg

Lynn Brock
Southwest Systems Technology

Clayton Carr
Lincoln Electric

Steve Chie Chong
Poseidon Innovation Sdn. Bhd.

Maya Chiesa
Lockheed Martin

Md Mahmudur Chowdhury
AMD

Joshua Colucci
Sheridan College

Paul Cooke
AGC

Ivan Cordova
Keytronic EMS

Kelly Dack
PCEA

Kimberly Daich
Cimetrix, Inc

Manuel Rene De los Santos Manjarrez
Valeo

Ted Ellefson
Seagate Technology

Cesar Escobedo
Omron Americas

Jules Fagbemiro

Steven Fernandes
KEMET Electronics

Joseph Fjelstad

Samuel Foo
MacdermidAlpha

James Fuller
Sanmina Corporation

Carolina Garcia
IBM

Nese Genētürk
EMT Elektronik Mühendislik San. Tic. Ltd. Sti

Mihaita Geoldes
Joyson Safety Systems

Jason Goodelle
Synaptics

Carmichael Gugliotti
MacDermid Alpha

David Hatch
Hatch Manufacturing Solutions

Joseph Hertline
Indium Corporation

Su-Chen Ho
Keysight Technologies

Michael Holan
Vario Systems

Michael Howard
Kimball Electronics Inc.

Yong Jia Hwang
Keysight Technology

Jorge Illingworth
Identco

Stanley Ingalsbe
Neptune Electronics Company, Inc.

Hong Jinki
LB semicon

Lee Jinkuk
LB semicon

Kurt Johnston
IDENTCO

Tom Katsioulas
Mentor, a Siemens Business

Manreet Kaur

Lip-Jing Khoo
Keysight Technologies

Shalaigh Koehl
IDENTCO International

Goh Kok
Dou Yee Enterprises (M) Sdn Bhd

Debbie Konrad
Aqueous Technologies

Zachary Langley
Ducommun Inc

Christopher Leone
AA Technology Inc

Sofia Limon
Samina

David Lopez

Chee Yean Low

Mark Lushell
SCS

Janet Lykowski
Nordson SONOSCAN

Miroslav Maramica
Area51 Electronics

Violeta Martinez
TURCK DUOTEC S DE RL DE CV

Sahana Marur Kempaiah
Rochester Institute of technology

Laura Mauer
Geer Mountain Software Corp

Kristen Mccutcheon
Keysight Tech

Elisa Mercado
Ducommun

Bob Miller
IDENTCO

Byungseok Min
XAVIS

Michael Murphy
The Morey Corp

Gobinath Nagalinggam
Cisco Systems

Kamil Nietupski
AA Technology Inc.

Trevor Norman
Axiomatique Technologies Inc

George Okada
Spectronix Corp.

Erick Ortega
Electromag

Ramanpreet Pahwa
I2R

Swagatika Patra
Binghamton University

Barbara Pauls
Mid America Taping and Reeling, Inc.

Oscar Paz
Valeo

Crystal Pereira

Steven Perng
Cisco Systems, Inc.

Jeffrey Perreira
Lutron Electronics Co., Inc.

Rattana Pongsawaree
Fabrinet West, Inc

Herb Post
TRADESAFE

Kumarabalan Pupalan
Venture Pintarmas Sdn Bhd

Jorge Quijano
REP0309296SA

Hector Rivera
Prime Technological Services, LLC

Jairus Adrian Roguel

Ryan Roudebush
CME

Herman Ruiz
Enphase Energy

Sergio Salazar Martinez

Malavarayan Sankarasubramanian

Zach Savana
Performance Technologies Group, Inc.

David Schneider
ConFab Services

NORMAN SCHWAB
NeoDenUSA

Dhrumil Shah
MacdermidAlpha

Menachem Shavit
Elbit Systems

Gaurav shitole
QEMS, Inc.

Matthew Siebenhuhner
MacDermid Alpha Electronics Solutions

Erik Sletten
FCT Assembly

Carrie Stevens

Biswajit Sur

Mario Talamantes
Stoneridge

Shantanu Tripathi
IIT Bombay

Julien Vieilledent
Thales Global Services

Mark Waterman
ECD

Jeffrey Wayne
NAS Electronics

Katie Worman
Identco

Austin Wright
Lockheed Martin

William Wright
Smiths Interconnect

Jizhe Yin
Philips Innovation Services

Joseph Ysasi
Brady Corporation

Kathy Zhao

Global Members

Amazon

Celestica, Inc.

Collins Aerospace

Creation Technologies Inc.

Henkel Electronic Materials LLC

HISCO, Inc.

IDENTCO

INVENTEC Performance Chemicals

ITW EAE

Juniper Networks

Keysight Technologies

KYZEN Corporation

L3HARRIS

MacDermid Alpha Electronics Solutions

Metallic Resources, Inc.

Micro Systems Technologies Management AG

NEO Technology Solutions

Nokia Bell Labs

Nordson Corporation

Plexus Corp.

Samtec

VEXOS

Zentech Manufacturing, Inc.

ZESTRON Americas

Corporate Members

4Front Solutions
Erie, Pennsylvania, USA

4Front Solutions
Palm Bay, Florida, USA

5N Plus Micro Powders
Montreal, Quebec, Canada

A. I. Technology Inc.
Princeton Jct., New Jersey, USA

AA Technology Inc.
Ronkonkoma, New York, USA

AB Electronics Inc
Brookfield, Connecticut, USA

AbelConn, LLC
New Hope, Minnesota, USA

ACC Electronix, Inc.
Normal, Illinois, USA

Accu-Automation Corporation
Waterloo, Ontario, Canada

Acculogic Inc.
Markham, Ontario, Canada

Accurate Technologies, Inc.
Novi, Michigan, USA

ACDi
Frederick, Maryland, USA

ACI Technologies, Inc.
Philadelphia, Pennsylvania, USA

ACL STATICIDE
Maple Grove, Minnesota, USA

Adam Electronics
Madison Heights, Michigan, USA

ADCO Circuits, Inc.
Rochester Hills, Michigan, USA

Advance Circuit Technology, Inc.
Rochester, New York, USA

Advanced Component Testing
Ronkonkoma, New York, USA

Aegis Software
Horsham, Pennsylvania, USA

AEIC
Litchfield, New Hampshire, USA

AGCO GRAIN & PROTEIN
St-Hubert, Canada

AGI Corporation
Huntsville, Alabama, USA

AIM - Soldadura de Mexico S.A. de C.V.
Juarez, CH, Mexico

AIM Solder
Cranston, Rhode Island, USA

Air Products and Chemicals, Inc.
Allentown, Pennsylvania, USA

Akrometrix LLC
Atlanta, Georgia, USA

Alan Woodford / NEO Technology Solutions
Westborough, Massachusetts, USA

All Flex Flexible Circuits
Bloomington, Minnesota, USA

Allendale Electronics Ltd.
Lockeport, Nova Scotia, Canada

Alliance Rubber Company
Hot Springs, Arkansas, USA

Alltemated
Wheeling, Illinois, USA

Altek Electronics, Inc.
Torrington, Connecticut, USA

Altron, Inc.
Anoka, Minnesota, USA

Altronic, LLC (A Member of the Hoerbiger Group)
Girard, Ohio, USA

Amazon
Kenmore, Washington, USA

Amazon
Sunnyvale, California, USA

Amazon Kunshan @ Compal Shanghai
Shanghai, Hong Kong

Amazon Lab126
Seattle, Washington, USA

Amazon Shenzhen
Shenzhen, Guangdong, China

Amazon Shenzhen @ ENSKY - CNSBG
Shenzhen, Guangdong, China

America II Electronics LLC
St. Petersburg, Florida, USA

American Hakko Products, Inc.
Valencia, California, USA

American Standard Circuits, Inc.
West Chicago, Illinois, USA

American Technology Components Inc.
Elkhart, Indiana, USA

Amitron Corporation
Elk Grove Village, Illinois, USA

Amkor Technology, Inc.
Tempe, Arizona, USA

Amphenol Borisch Technologies
Grand Rapids, Michigan, USA

Ampthink
Garland, Texas, USA

Analog Technologies Corporation
Burnsville, Minnesota, USA

ANDA TECHNOLOGIES USA INC
Fremont, California, USA

Annapolis Micro Systems, Inc.
Annapolis, Maryland, USA

AOI SYSTEMS
Davenport, Florida, USA

APAG Elektronik
Windsor, Ontario, Canada

Apollo Seiko
Bridgman, Michigan, USA

Apollos Industries
Orange, California, USA

Appareo
Fargo, North Dakota, USA

Applicad Inc.
Farmingdale, New Jersey, USA

Aqueous Technologies
Corona, California, USA

Arc-Tronics, Inc.
Elk Grove Village, Illinois, USA

Argo Transdata
Clinton, Connecticut, USA

Ascentec Engineering
Tualatin, Oregon, USA

Ascentron, Inc
White City, Oregon, USA

ASM Assembly Systems
Suwanee, Georgia, USA

Astronautics Corporation of America
Milwaukee, Wisconsin, USA

ASYS Group Americas Inc.
Suwanee, Georgia, USA

Austin American Technology Corporation
Burnet, Texas, USA

Axiom Electronics LLC
Hillsboro, Oregon, USA

Axiomatique Technologies Inc
Fremont, California, USA

Bare Board Group
Largo, Florida, USA

BBM, Inc.
McKinney, Texas, USA

Benchmark Electronics, MN Division
Winona, Minnesota, USA

Bently Nevada LLC
Minden, Nevada, USA

BEST Inc.
Rolling Meadows, Illinois, USA

Better Board Buying
Indian Rocks Beach, Florida, USA

BGA Test & Technology
Bohemia, New York, USA

Bittele Electronics Inc.
Markham, Ontario, Canada

BlueRing Stencils
Lumberton, New Jersey, USA

Brady Corporation
Milwaukee, Wisconsin, USA

BSE INC
Schaumburg, Illinois, USA

BTU International
North Billerica, Massachusetts, USA

BTW Inc.
Coon Rapids, Minnesota, USA

Burton Industries, Inc.
Hazelhurst, Wisconsin, USA

CalcuQuote
Muphy, Texas, USA

CAMtek, Inc.
Bloomington, Illinois, USA

Canon USA, Inc.
San Jose, California, USA

CareHawk Inc.
Kitchener, Ontario, Canada

Carlton Industries Corporation
Hamden, Connecticut, USA

CCL Design
Wheaton, Illinois, USA

Celestica Electronics (M) Sdn. Bhd.
Senai, Johor, Malaysia

Celestica Inc.
Suzhou, Jiangsu, China

Celestica Inc.
Singapore, Singapore

Celestica Inc.
Sriracha, Chon Buri, Thailand

Celestica, Inc.
Toronto, Ontario, Canada

Celestica, Inc.
North York, Ontario, Canada

CEMSI
Weyers Cave, Virginia, USA

CheckSum LLC
Arlington, Washington, USA

Chem Logic
Austin, Texas, USA

Cimetrix, Inc
Salt Lake City, Utah, USA

Circuit Check Inc.
Maple Grove, Minnesota, USA

Circuit Works Corporation
Waukegan, Illinois, USA

CO-AX Technology, Inc.
Solon, Ohio, USA

Colibri Circuits
Cave Creek, Arizona, USA

Collins Aerospace
Bengaluru, Karnataka, India

Collins Aerospace
Rockford, Illinois, USA

Collins Aerospace
Melbourne, Florida, USA

Collins Aerospace
Cedar Rapids, Iowa, USA

Colonial Electronic Manufacturers Inc.
Nashua, New Hampshire, USA

Communications Security Establishment
Ottawa, Ontario, Canada

Computrol Meridian
Meridian, Idaho, USA

Comtech PST
Melville, New York, USA

Comtest Networks Inc.
Ottawa, Ontario, Canada

Comtree Inc.
Mississauga, Ontario, Canada

Condair Inc.
Sturtevant, Wisconsin, USA

Conductive Containers
New Hope, Minnesota, USA

Conecsus LLC
Terrell, Texas, USA

Conecsus LLc Mexico
Mexico

Conformance Technologies
Monroeville, Pennsylvania, USA

Contemporary Controls
Downers Grove, Illinois, USA

Contract Manufacturing Consultants, Inc.
Bothell, Washington, USA

ControlTek
Vancouver, Washington, USA

Cornet Technology
Springfield, Virginia, USA

Count-On Tools, Inc.
Gainesville, Georgia, USA

CPAC Systems AB
NA Molndal, Sweden

Crane Aerospace and Electronics
Lynnwood, Washington, USA

Creation Technologies Inc.
Markham, Ontario, Canada

Creative Electron, Inc.
San Marcos, California, USA

CRM Synergies Mexico S.A de CV
Ciudad de Mexico, Mexico

Crown Equipment Corporation
New Bremen, Ohio, USA

Crystal Mark, Inc.
Glendale, California, USA

Cumberland Electronics
Harrisburg, Pennsylvania, USA

CyberOptics Corporation
Minneapolis, Minnesota, USA

Daktronics, Inc.
Brookings, South Dakota, USA

Datest Corporation
Fremont, California, USA

Datum Alloys
Binghamton, New York, USA

DCA Manufacturing Corporation
Cumberland, Wisconsin, USA

DEKRA iST Reliability Services Inc.
Hsinchu City, Taiwan

DEN-ON INSTRUMENTS CO., LTD
Tokyo, Japan

DG Marketing Corporation
Austin, Texas, USA

Dimation
Shakopee, Minnesota, USA

Dorigo Systems Ltd.
Burnaby, British Columbia, Canada

Ducommun Incorporated
Tulsa, Oklahoma, USA

DYCONEX AG
Bassersdorf, Germany

DYCONEX AG
Bassersdorf, Zurich, Switzerland

Dynalab, Inc.
Reynoldsburg, Ohio, USA

E.T.S. Group, Inc.
Lake Forest, California, USA

Eastek International Corporation
Lake Zurich, Illinois, USA

ECD
Milwaukie, Oregon, USA

EEI Manufacturing Services
Clearwater, Florida, USA

EI Microcircuits, Inc.
Mankato, Minnesota, USA

ELANTAS PDG, Inc.
St Louis, Missouri, USA

Elbit Systems
Israel

Electro Tech Systems
Glenside, Pennsylvania, USA

Electrolab, Inc.
Boerne, Texas, USA

Electronic Assembly Products
Dayton, Ohio, USA

Electronic Interconnect
Elk Grove Village, Illinois, USA

Electronic Systems, Inc.
Sioux Falls, South Dakota, USA

Ellsworth Adhesives
Germantown, Wisconsin, USA

Eltek USA Inc.
Manchester, New Hampshire, USA

Emerson Machine Automation Solutions
Charlottesville, North Carolina, USA

EMT Elektronik Mühendislik San. Tic. Ltd. Sti
Turkey

ENGENT
Norcross, Georgia, USA

Engent, Inc.
Norcross, Georgia, USA

EO Technics International, Inc
Gilbert, Arizona, USA

Epec
New Bedford, Massachusetts, USA

Epoxy Technology Inc.
Billerica, Massachusetts, USA

EPTAC Corporation
Manchester, New Hampshire, USA

ESSEMTEC USA
Pitman, New Jersey, USA

E-tronix
St Louis Park, Minnesota, USA

Europlacer Americas'
Tampa, Florida, USA

EV Group, Inc.
Tempe, Arizona, USA

Excel Electronics Inc
Elkhart, Indiana, USA

Exceltech Inc
McMinnville, Oregon, USA

Express Manufacturing Inc.
Santa Ana, California, USA

Extant Aerospace
Melbourne, Florida, USA

FHP Reps
Granbury, Texas, USA

Finetech
Gilbert, Arizona, USA

FINN Test Electronics
Lake Zurich, Illinois, USA

Firstronic LLC
Grand Rapids, Michigan, USA

FKN Systek, Inc.
Millis, Massachusetts, USA

Flex
Zapopan, JA, Mexico

Flexible Circuits, Inc.
Warrington, Pennsylvania, USA

FlexLink Systems, Inc.
Allentown, Pennsylvania, USA

Foresite, Inc.
Kokomo, Indiana, USA

FreeWave Technologies
Boulder, Colorado, USA

Fuji America Corporation
Vernon Hills, Illinois, USA

Fujitsu Networks Comunications

Fusion EMS
Hillsboro, Oregon, USA

Gables Engineering Inc
Coral Gables, Florida, USA

Garland Service Company
Garland, Texas, USA

Garmin AT, Inc.
Salem, Oregon, USA

Garmin International
Olathe, Kansas, USA

GEN3 Systems
Farnborough, United Kingdom

General Microcircuits Inc.
Mooresville, North Carolina, USA

General Monitors, Inc.
Lake Forest, California, USA

Gesick Consulting and Materials
OLD SAYBROOK, Connecticut, USA

GHSP
Grand Haven, Michigan, USA

Glenbrook Technologies Inc.
Randolph, New Jersey, USA

Google
Mountain View, California, USA

GPD Global
Grand Junction, Colorado, USA

Great Lakes Engineering
Maple Grove, Minnesota, USA

GreenSoft Technology, Inc.
Pasadena, California, USA

Guild Manufacturing Solutions LLC
Oviedo, Florida, USA

Hangzhou H3C Tech. Co., Ltd.
Hangzhou, Zhejiang Province, China

Hanwha Techwin Automation Americas. Inc.
Cypress, California, USA

Harimatec Inc.
Duluth, Georgia, USA

Harman de Mexico S de RL de CV
Queretaro, Mexico

Henkel
Rocky Hill, Connecticut, USA

Henkel
Irvine, California, USA

Henkel Electronic Materials
Irvine, California, USA

Henkel Electronic Materials
Rocky Hill, Connecticut, USA

Henkel Electronic Materials LLC
Chanhassen, Minnesota, USA

Henkel Electronic Materials LLC
Irvine, California, USA

Henkel Electronics
Hertfordshire, UK

Henkel Electronics
Herts,

Henkel Electronics Inc.
Irvine, California, USA

Henkel US Operations Corp.
Prescott, Wisconsin, USA

Hentec Industries Inc.
Otis Orchards, Washington, USA

HISCO, Inc.
Somerset, New Jersey, USA

HISCO, Inc.
Westminster, Colorado, USA

HISCO, Inc.
Houston, Texas, USA

HISCO, Inc.
Franklin, Massachusetts, USA

HISCO, Inc.
San Diego, California, USA

HISCO, Inc.
Buford, Georgia, USA

HISCO, Inc.
Austin, Texas, USA

HISCO, Inc.
Corona, California, USA

Hi-Tek Electronics
Salem, Oregon, USA

Honeywell FM&T
Kansas City, Missouri, USA

Houstech, Inc.
Houston, Texas, USA

Hughes Circuits, Inc.
San Marcos, California, USA

HumiSeal Europe Ltd.
Winnersh, United Kingdom

HZO
Burlington, North Carolina, USA

I Source Technical Services, Inc.
Lake Forest, California, USA

IBM Canada Ltée
Bromont, Quebec, Canada

iBtest Innovative Board Test
Tlaquepaque, Mexico

IDENTCO
Ingleside, Illinois, USA

IDENTCO
San Jose, California, USA

IDENTCO Europe
Hanau, Germany

IDENTCO International
Grayslake, Illinois, USA

IKEUCHI USA, INC.
Cincinnati, Ohio, USA

IMI, Inc.
Haverhill, Massachusetts, USA

INAC US, Inc.
Torrance, California, USA

Indium Corporation
Utica, New York, USA

INGUN USA, Inc.
Clover, South Carolina, USA

Innovation Machine, Ltd
Helena, Montana, USA

Innovative Circuits, Inc.
Alpharetta, Georgia, USA

Inovar, Inc.
North Logan, Utah, USA

Inovaxe Corporation
Deerfield Beach, Florida, USA

InsulFab PCB Tooling
Spartanburg, South Carolina, USA

Integrated Technology Limited
Markham, Ontario, Canada

Intel Corporation
Hillsboro, Oregon, USA

International Control Services, Inc.
Decatur, Illinois, USA

INVENTEC Performance Chemicals
Bruges, France

INVENTEC Performance Chemicals
Vincennes, France

IPS Assembly Corporation
Livonia, Michigan, USA

IPTE, LLC
Alpharetta, Georgia, USA

Isola Group
Jefferson, Ohio, USA

iST-Integrated Service Technology Inc.
Hsinchu, Taiwan

ITM Consulting
Springfield, Tennessee, USA

Itron, Inc.
Waseca, Minnesota, USA

ITW Contamination Control
Kennesaw, Georgia, USA

ITW EAE
Oosterhout, Netherlands

ITW EAE
Singapore, Singapore

ITW EAE
Yulee, Florida, USA

ITW EAE
Camdenton, Missouri, USA

ITW EAE
Hopkinton, Massachusetts, USA

ITW EAE
Lakeville, Minnesota, USA

ITW EAE
Hopkinton, Missouri, USA

ITW EAE
New Boston, New Hampshire, USA

J.W. Speaker
Germantown, Wisconsin, USA

Jabil Circuit, Inc.
St. Petersburg, Florida, USA

JBC Tools USA Inc.
SAINT LOUIS, Missouri, USA

Jendco Technologies
Fort Wayne, Indiana, USA

JH Technologies
Fremont, California, USA

JJ Technologies
Wareham, Massachusetts, USA

John Deere Electronic Solutions, Inc.
Fargo, North Dakota, USA

Juniper Networks
Shanghai, China

Juniper Networks
Bangalore-Karnataka, India

Juniper Networks
Kuala Lumpur, Malaysia

Juniper Networks
Westford, Massachusetts, USA

Juniper Networks
Sunnyvale, California, USA

Juniper Networks
Fremont, California, USA

K & F Electronics, Inc.
Fraser, Michigan, USA

Kapsch TrafficCom
Mississauga, Ontario, Canada

Kentzy International, Inc.
Allen, Texas, USA

Keysight Technologies
ChengDu, Sichuan, China

Keysight Technologies
Boeblingen, Germany

Keysight Technologies
Georgetown, Penang, Malaysia

Keysight Technologies
Bayan Lepas, Penang, Malaysia

Keysight Technologies
Tlaquepaque, Mexico

Keysight Technologies
Yishun, Singapore

Keysight Technologies
Edinburgh, UK

Keysight Technologies
Santa Clara, California, USA

Keysight Technologies
Colorado Springs, Colorado, USA

Keysight Technologies
Santa Rosa, California, USA

Keysight Technologies International
Gurgaon, India

Keytronic
Oakdale, Minnesota, USA

KIC
San Diego, California, USA

Kimball Electronics Inc.
Jasper, Indiana, USA

Koh Young
Duluth, Georgia, USA

Koh Young Technology Inc.
Geumcheon-Gu, Seoul, Korea, South

Koki Solder America Inc.
Lake Elsinore, California, USA

kolb CLEANING TECHNOLOGY GmbH
Willich, Germany

Kostal Ireland GMBH
Abbeyfeale, Co. Limerick, Ireland

Krayden, Inc.
Denver, Colorado, USA

Krypton Solutions
Plano, Texas, USA

Kulicke & Soffa Industries
Fort Washington, Pennsylvania, USA

Kurt Whitlock Associates
St. Cloud, Florida, USA

Kurtz Ersa, Inc.
Plymouth, Wisconsin, USA

KYZEN Corporation
Nashville, Tennessee, USA

KYZEN Corporation
Schwenksville, Pennsylvania, USA

KYZEN Corporation
Atlanta, Georgia, USA

KYZEN Corporation
Broadlands, Virginia, USA

L3HARRIS
Rochester, New York, USA

LEL Semi
Duncan, South Carolina, USA

Lenze
Uxbridge, Massachusetts, USA

Lexicon Technologies Inc
Conyers, Georgia, USA

Libra Industries, Inc.
Mentor, Ohio, USA

Lockheed Martin
Oldsmar, Florida, USA

Lockheed Martin
Owego, New York, USA

Logic PD, Inc.
Eden Prairie, Minnesota, USA

Logican Technologies
Edmonton, Alberta, Canada

LPKF Laser & Electronics
Tualatin, Oregon, USA

MacDermid Alpha
Waterbury, Connecticut, USA

MacDermid Alpha Electronics Solutions
Sao Bernardo do Campo, Sao Paulo, Brazil

MacDermid Alpha Electronics Solutions
Bangalore, India

MacDermid Alpha Electronics Solutions
Schertz, Texas, USA

MacDermid Alpha Electronics Solutions
Waterbury, Connecticut, USA

MacDermid Alpha Electronics Solutions
Drexel Hill, Pennsylvania, USA

MacDermid Alpha Electronics Solutions
Somerset, New Jersey, USA

MacDermid Enthone Electronic Solutions
Waterbury, Connecticut, USA

Mack Technologies Inc.
Melbourne, Florida, USA

Magnalytix
Nashville, Tennessee, USA

MAHA SOLUCIONES INTEGRALES PARA LA INDUSTRIA
Reynosa, Mexico

Manncorp
Huntingdon Valley, Pennsylvania, USA

Maqim SA de CV
Tlajomulco de Zuñiga, JA, Mexico

Maquiladora de Servicios MMS Sa de CV
Mexico

Master Bond Inc.
Hackensack, New Jersey, USA

Matric LTD
Seneca, Pennsylvania, USA

MEC A/S
Ballerup, Denmark

MELECS Electronics Queretaro
Queretaro, Queretaro, Mexico

Metallic Resources, Inc.
Twinsburg, Ohio, USA

MG Chemicals
Burlington, Ontario, Canada

Micro Systems Engineering GmbH
Berg, Germany

Micro Systems Engineering, Inc.
Lake Oswego, Oregon, USA

Micro Systems Technologies Management AG
Baar, Switzerland

Micro Systems Technologies, Inc.
Plano, Texas, USA

Micro Systems Technologies, Inc.
Brookfield, Connecticut, USA

MicroCare Corporation
New Britain, Connecticut, USA

Micron Corporation
Norwood, Massachusetts, USA

MicroScreen, LLC
South Bend, Indiana, USA

Microsoft Corporation
Redmond, Washington, USA

Micross Components, LLC
Manchester, New Hampshire, USA

Mid America Taping and Reeling, Inc.
Glendale Heights, Illinois, USA

Mid-America Taping & Reeling
Glendale Heights, Illinois, USA

Mirac, LLC.
Lynchburg, Ohio, USA

Miraco, Incorporated
Manchester, New Hampshire, USA

Mirtec Corporation
Oxford, Connecticut, USA

MPI
Seymour, Connecticut, USA

MPL Inc.
Ithaca, New York, USA

Mudisa Sa De CV
Tlajomulco de Zuniga, Jalisco, Mexico

Multicircuits Inc.
Oshkosh, Wisconsin, USA

Murray Percival Company
Auburn Hills, Michigan, USA

M-Wave International, LLC
Glendale Heights, Illinois, USA

Mycronic, Inc
Rowley, Massachusetts, USA

N.F. Smith & Associates, L.P.
Houston, Texas, USA

NAS Electronics
Las Vegas, Nevada, USA

National Circuit Assembly
Garland, Texas, USA

National Instruments
Austin, Texas, USA

NEO Technology Solutions
Chih. MX, JA, Mexico

NEO Technology Solutions
Aurora, Illinois, USA

NEO Technology Solutions
Omro, Wisconsin, USA

NEO Technology Solutions
Longmont, Colorado, USA

NEO Technology Solutions (OnCore Manufacturing, LLC)
Westborough, Massachusetts, USA

Neoden USA
Ringwood, New Jersey, USA

Niche Electronics Technologies LLC.
Shippensburg, Pennsylvania, USA

Nihon Superior Company, Ltd.
Suita City, Osaka, Japan

Nikon Metrology, Inc.
Brighton, Michigan, USA

Nokia
Ottawa, Ontario, Canada

Nokia
Oulu, Finland

Nokia
Plano, Texas, USA

Nokia
Oklahoma, Oklahoma, USA

Nokia
Murray Hill, New Jersey, USA

Nokia Bell Labs
Murray Hill, New Jersey, USA

Nokia Canada
Ottawa, Ontario, Canada

Nokia Siemens Networks
Espoo, Finland

Norcott Technologies Ltd
Widnes,

Nordson ASYMTEK
Carlsbad, California, USA

Nordson DAGE
Aylesbury, Buckinghamshire, Bucks, UK

Nordson EFD
East Providence, Rhode Island, USA

Nordson SELECT
Liberty Lake, Washington, USA

Nordson SONOSCAN
Elk Grove Village, Illinois, USA

Northrop Grumman
Salt Lake City, Utah, USA

NPI Services, Inc.
Costa Mesa, California, USA

NPI Technologies, Inc.
Sugar Land, Texas, USA

NRI Electronics (division of ECI)
Anoka, Minnesota, USA

nScrypt
Orlando, Florida, USA

NTS-Baltimore
Hunt Valley, Maryland, USA

Nu-Way Electronics, Inc.
Elk Grove Village, Illinois, USA

nVidia Corporation
Yokneam, Israel

Odyssey Electronics, Inc.
Livonia, Michigan, USA

OES Inc.
London, Ontario, Canada

Omron Inspection Systems
Hoffman Estates, Illinois, USA

Optimal Electronics Corporation
Austin, Texas, USA

OSDA Contract Services
Milford, Connecticut, USA

Out of the Box Manufacturing
Renton, Washington, USA

P. Kay Metal, Inc.
Los Angeles, California, USA

PA&LS, LLC
Trabuco Canyon, California, USA

PAC Global, Inc.
Dallas, Texas, USA

PAC Mexico
Guadalajara, JA, Mexico

PACE Worldwide
Vass, North Carolina, USA

PacTech USA Inc.
Santa Clara, California, USA

Palomar Technologies
Carlsbad, California, USA

PalPilot International Corporation
Englewood, Colorado, USA

PARMI USA INC.
San Diego, California, USA

Parpro Technologies
Santa Ana, California, USA

PCB Connect Inc.
Sharon, Massachusetts, USA

PCBA Supplies
Anna, Texas, USA

PDR Rework and Test Systems
Shingle Springs, California, USA

Peerless Instrument
East Farmingdale, New York, USA

Pennatronics Corporation
California, Pennsylvania, USA

Pentagon EMS Corporation
Hillsboro, Oregon, USA

Performance Technologies Group, Inc.
Tyngsboro, Massachusetts, USA

PFC Flexible Circuits
Mississiauga, Ontario, Canada

PFC Flexible Circuits
Lexington, Massachusetts, USA

Photo Etch Technology, Inc.
Lowell, Massachusetts, USA

Pillarhouse USA, Inc.
Elk Grove, Illinois, USA

Pivot-DigitTron, Inc.
Shawnee, Kansas, USA

Plexus
Penang, Malaysia

Plexus
Zapopan-JAL, Mexico

Plexus Corp.
Neenah, Wisconsin, USA

Plexus Corp.
Buffalo Grove, Illinois, USA

Plexus Corp.
Neenah, Colorado, USA

Plexus Corp. (UK) Ltd.
Kelso, Roxburghshire,

Plexus Kelso
Kelso,

Plexus Manufacturing Sdn. Bhd.
Bayan Lepas, Penang, Malaysia

Polyonics
Westmoreland, New Hampshire, USA

Powell Industries, Inc.
Highland, Utah, USA

Powertrain Control Solutions
Ashland, Virginia, USA

Practical Components
Los Alamitos, California, USA

Precision PCB Services, Inc.
Oroville, California, USA

Precision Technology, Inc.
Plano, Texas, USA

PRIDE Industries
Roseville, California, USA

Prime Technological Services, LLC
Suwanee, Georgia, USA

Pro-Active Engineering, Inc.
Sun Prairie, Wisconsin, USA

ProActive Process Solutions Group
Bastrop, Texas, USA

Process Sciences, Inc.
Leander, Texas, USA

Promex Industries, Inc.
Santa Clara, California, USA

Prototron Circuits
Redmond, Washington, USA

PVA
Cohoes, New York, USA

QSC, LLC
Costa Mesa, California, USA

QUALITEK INTERNATIONAL, INC.
Addison, Illinois, USA

Qual-Pro Corporation
Gardena, California, USA

Quiptech
Tlajomulco de Zuï¿½iga, Mexico

Rauland-Borg Corporation
Mount Prospect, Illinois, USA

Raven Industries Inc.
Sioux Falls, South Dakota, USA

RBB Systems
wooster, Ohio, USA

Rehm Thermal Systems LLC
Roswell, Georgia, USA

Reliable Controls Corporation
Victoria, British Columbia, Canada

Renishaw PLC
Chippenham, Wiltshire,

Repstronics
Zapopan, JA, Mexico

Retronix
Coatbridge, Lanarkshire, UK

RiverSide Electronics Ltd.
Lewiston, Minnesota, USA

Robert McKeown Company, Inc.
Branchburg, New Jersey, USA

Robotas Technologies Ltd
Harrogate, UK

Rochester Institute of Technology (RIT)
Rochester, New York, USA

Rocktin Technology Canada
Richmond, British Columbia, Canada

Rockwell Automation
Mayfield Heights, Ohio, USA

Rockwell Automation
Mequon, Wisconsin, USA

Rogers Electro-Matics
Syracuse, Indiana, USA

Safari Circuits, Inc.
Otsego, Michigan, USA

Saki America Inc.
Fremont, California, USA

Saline Lectronics, Inc.
Saline, Michigan, USA

Samtec
R.L. Alajuela, Costa Rica

Samtec
Mechanicsburg, Pennsylvania, USA

Samtec
New Albany, Indiana, USA

Samtec
Melbourne, Florida, USA

Samtec
Lutz, Florida, USA

Samtec
Dacula, Georgia, USA

Samtec Microelectronics
Colorado Springs, Colorado, USA

Sanmina Corporation
Huntsville, Alabama, USA

ScanCAD International
Morrison, Colorado, USA

ScanCAD International, Inc.
Conifer, Colorado, USA

SCHUNK Electronic Solutions
Morrisville, North Carolina, USA

SCHUNK Mexico
Queretaro, Mexico

Schweitzer Engineering Labs
Pullman, Washington, USA

Scienscope
Chino, California, USA

Scott Electrokrafts, Inc.
Andover, Connecticut, USA

SCS
USA

Seagate Technology
Shakopee, Minnesota, USA

SEHO North America, Inc.
Erlanger, Kentucky, USA

Seica Inc.
Haverhill, Massachusetts, USA

Seika Machinery, Inc.
Torrance, California, USA

Semi-Kinetics
Lake Forest, California, USA

Senju Comtek Corporation
Santa Clara, California, USA

SHENMAO Technology, Inc.
San Jose, California, USA

SICK, Inc.
Minneapolis, Minnesota, USA

Sigmapoint Technologies Inc.
Cornwall, Ontario, Canada

Simplimatic Automation
Virginia, Virginia, USA

SMART Microsystems
Elyria, Ohio, USA

Smart Sonic
Cleveland, Ohio, USA

Smart Splice, LLC
Surfside Beach, South Carolina, USA

SMarTsol Technologies
Zapopan, Jalsico, Mexico

SMT North America, Inc.
Richmond, Virginia, USA

SMT Worldwide
Santa Catarina, Nuevo Leon, Mexico

SMTC
Melbourne, Florida, USA

SMTo Engineering
Tlaquepaque, JA, Mexico

SMTVYS LLC
El Paso, Texas, USA

SMTXTRA USA INC
Maryville, Tennessee, USA

SolarEdge Technologies
Herzeliya, Israel

Solder Indonesia, PT.
Cileungsi - Bogor, Indonesia

SolderMask, Inc.
Huntington Beach, California, USA

SolderStar LLC
Clearwater, Florida, USA

Southwest Research Institute
San Antonio, Texas, USA

Sparton Onyx
Watertown, South Dakota, USA

SPEA America
Tyler, Texas, USA

SPEA SpA
Volpiano, Italy

Spectra-Tech Manufacturing Inc
Batavia, Ohio, USA

Spectrum AMT
Colorado Springs, Colorado, USA

Speedprint Technology
Tampa, Florida, USA

SRC Tec
N Syracuse, New York, USA

Stanley Healthcare
Lincoln, Nebraska, USA

StaticStop a division of SelecTech, Inc.
Avon, Massachusetts, USA

StenTech, Inc.
GOLDEN, Colorado, USA

STI Electronics, Inc.
Madison, Alabama, USA

STIM Canada Inc.
Toronto, Ontario, Canada

Streamline Circuits LLC
Santa Clara, California, USA

Streamline Electronic Manufacturing

Sunshine Global Circuits
Plano, Texas, USA

Super PCB
Plano, Texas, USA

Superior Flux & Manufacturing
Solon, Ohio, USA

Surf-Tech Manufacturing Corp
Ronkonkoma, New York, USA

Surtek Industries Inc.
Surrey, British Columbia, Canada

SVTronics, Inc.
Plano, Texas, USA

Synapse Electronique Inc.
Shawinigan, Quebec, Canada

Syncro Corp
Arab, Alabama, USA

SynQor Inc
Boxborough, Massachusetts, USA

Sypris Electronics, LLC
Tampa, Florida, USA

Systems Innovation Engineering
Mullica Hill, New Jersey, USA

TAGARNO USA
Greenwood, South Carolina, USA

Technica, USA
San Jose, California, USA

Technical Support Inc.
Omaha, Nebraska, USA

Technimark, Inc.
Cary, Illinois, USA

Techtron Systems Inc.
Sohon, Ohio, USA

Tecnova Electronics Inc.
Waukegan, Illinois, USA

Tek PAk, Inc.
Batavia, Illinois, USA

Tektronix, Inc.
Beaverton, Oregon, USA

Teligent Ems
USA

Teradyne, Inc.
N. Reading, Massachusetts, USA

Test Research, Inc.
Taipei, TA, Taiwan

Test Technology Associates
Carrollton,, Texas, USA

Texmac/Takaya, Inc.
McHenry, Illinois, USA

The ECM Group, LLC
Clayton, Missouri, USA

The Jefferson Project
Orlando, Florida, USA

The Morey Corp
Woodridge, Illinois, USA

The Test Connection, Inc.
Hunt Valley, Maryland, USA

Thermaltronics USA, Inc.
Great Neck, New York, USA

Tintronics
Huntsville, Alabama, USA

TopLine
Milledgeville, Georgia, USA

TORONTRONICS CIRCUIT TECHNOLOGY INC.
Toronto, Ontario, Canada

TouchPad Electronics LLC
Mukwonago, Wisconsin, USA

Tracer Inc.
Golden, Colorado, USA

TRADESAFE
Wichita, Kansas, USA

Trans Tec America
Chandler, Arizona, USA

Transforming Technologies
Toledo, Ohio, USA

Transition Automation, Inc.
Massachusetts, USA

Trenton Technology Inc.
Utica, New York, USA

Trilogy Circuits, Inc.
Richardson, Texas, USA

TROIKA Latin America
McAllen, Texas, USA

TruStar
Brentwood, Tennessee, USA

TURCK DUOTEC S DE RL DE CV
Arteaga, Coahuila, Mexico

U-Bond Material Technology Co. Ltd.
Donguan City, China

Ultimate Solutions
Cypress, Texas, USA

UltraTape
WIlsonville, Oregon, USA

Unison Industries
Jacksonville, Florida, USA

Universal Avionics
Tucson, Arizona, USA

Universal Instruments Corporation
Conklin, New York, USA

USM Reps
El Paso, TX, Mexico

Valtronic Technologies (USA) Inc.
Solon, Ohio, USA

Variosystems, Inc.
Southlake, Texas, USA

Venkel Ltd.
Austin, Texas, USA

Verion Training Systems
Dallas, Texas, USA

Versa Electronics
Minneapolis, Minnesota, USA

VEXOS
Markham, Ontario, Canada

VEXOS
Dongguan City, Guangdong, PRC, China

VEXOS
Shenzhen, Guangdong, China

VEXOS
LaGrange, Ohio, USA

VEXOS - LaGrange
LaGrange, Ohio, USA

Virtual Industries Inc.
Colorado Springs, Colorado, USA

Viscom
Zapopan, Jalisco, Mexico

Viscom Inc.
Duluth, Georgia, USA

VisiConsult X-Ray Solutions America Corp.
Atlanta, Georgia, USA

Vision Engineering
New Milford, Connecticut, USA

Vitrox
Penang, Malaysia

VJ Electronix, Inc.
Chelmsford, Massachusetts, USA

V-TEK, Inc.
Mankato, Minnesota, USA

WAGO CORPORATION
Germantown, Wisconsin, USA

Warton Metals Ltd
Haslingden, UK

Watchfire Signs
Danville, Illinois, USA

Weller Tools
Lexington, South Carolina, USA

WinTronics, Inc.
Sharon, Pennsylvania, USA

Wittco Sales, Inc.
Murrieta, California, USA

WORLD Electronics
Reading, Pennsylvania, USA

Yamaha
Kennesaw, Georgia, USA

Yield Engineering Systems
Fremont, California, USA

Yxlon International
Hudson, Ohio, USA

Zentech Manufacturing
Parkville, Maryland, USA

Zentech Manufacturing, Inc.
Baltimore, Maryland, USA

ZESTRON Americas
Manassas, Virginia, USA

ZESTRON Corporation
Minhang District, Shanghai, China

ZESTRON Corporation
Ingolstodt, Germany

ZESTRON Corporation
Koza-gun, Kanagawa, Japan

ZESTRON Corporation
Prai, Penang, Malaysia

ZESTRON Corporation
Manassas, Virginia, USA

ZESTRON Corporation
Minneapolis, Minnesota, USA

ZESTRON Mexico
Zapopan, JA, Mexico

Zollner Electronics Inc.
Milpitas, California, USA

Zymet, Inc.
East Hanover, New Jersey, USA

6600 City West Parkway, Suite 300
Eden Prairie, MN 55344 USA

Phone: +1-952-920-7682
Fax: +1-952-926-1819

E-Mail: smta@smta.org
Web site: www.smta.org