RELIABILITY AND PERFORMANCE OF WAFER LEVEL FAN OUT PACKAGE FOR AUTOMOTIVE RADAR

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ABSTRACT

Embedded wafer level ball grid array (eWLB) or Fan-out wafer-level packaging (FO-WLP) is investigated as a package for Monolithic Microwave Integrated Circuit (MMICs) for automotive radar applications in the 77GHz range. Special focus is put on the thermo-mechanical performance to achieve automotive quality targets. The typical fatigue modes "solder ball fatigue" and "copper fatigue", evolving during thermo-mechanical stress like cycling on board will be discussed. Simulation as well as experimental preparation results for typical fatigue levels are given. In addition, several influencing parameters are listed and rated regarding their effectiveness. The theoretical framework why solder ball fatigue is the only failure mode causing electrical failure is provided.

The impact of different thermo-mechanically driven fatigue modes is discussed. Two important parameters to be considered for the functionality of the Radar system are Radio Frequency (RF) and thermal performance.

For elaborating the RF performance with present fatigue modes, the phase shift between different channels and pads is analyzed by full-wave electromagnetic (EM) simulation. It is found that for fatigue levels up to 90% the phase shift stays below specification for single fatigue modes and may approach specification only for an unlikely combination of all 90% fatigue modes.

For assessing the thermal performance with present fatigue modes, thermal simulation as well as thermal measurements are used. Assuming 50% degradation in average for all thermal balls, an increase of the thermal resistance (Rth) of up to about 30% is seen. On average for all thermal measurements, the deviation between measurement and simulation is within $\Delta T = \pm 1°C$.

Key words: Automotive Radar, eWLB, FO-WLP, MMIC, Reliability, Fatigue

INTRODUCTION

Automotive Radar technology at 77GHz for Advanced Driver Assistance Systems (ADAS) and autonomous driving requires a package solution, which provides both superior RF performance and fulfills the strict automotive reliability requirements. In the past, the automotive industry used predominantly very mature semiconductors and packages. However, today a car will need to use the latest packaging technology to provide the best solution for ADAS sensors. One example for this trend is the eWLB package. Infineon was the first company introducing the new and emerging eWLB package technology to the automotive market in 2012 [1], only 3 years after introducing this technology to the consumer market, also by Infineon [2] [3].

Characteristic to eWLB package technology is the signal routing directly on top of the silicon device and package body by using thin dielectric layers for electrical insulation and thin copper film layers for electrical redistribution. Frontend Si-technologies and processes became standard for this backend package technology. These offer low parasitic inductances, shorter signal pathways and together with more freedom in designing the layout of the redistribution layers (RDL), thus an excellent RF transition.

Today this low-cost wafer-level eWLB packaging solution with its attractive RF performance is now used in the second generation for automotive Radar technologies of Infineon [4] [5] and is also widely spread and used by others for many automotive Radar systems for 77GHz [6]-[8]. Please refer to [9]-[12] for more details, schematics and cross-sections of the eWLB package.

In the following, we describe how the eWLB technology fulfills the demanding performance and reliability requirements of automotive radar sensors. Three important topics will be addressed:

I. Thermo-mechanical behavior (what drives thermo-mechanical lifetime behavior and what fatigue modes do we have?)

II. RF performance (what will impact the RF-performance?)

III. Thermal performance (how to setup thermal management and what will change thermal behavior?).

I. THERMO-MECHANICAL BEHAVIOR

eWLB with the short interconnection means there is no material layer at the package side, which is able to buffer any coefficient of thermal expansion (CTE) mismatch. The solder balls are exposed to the full CTE mismatch between the printed circuit board (PCB) and the eWLB's main components (silicon and molding compound).

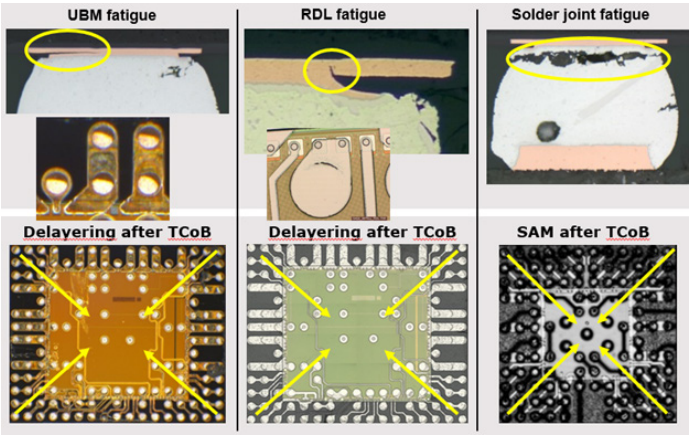

Figure 1: X-Section images of thermally stressed 2nd level solder joints and the evolved typical fatigue modes. SAM-image and images of chemical delayered dies reveal radial orientation of the fatigue modes w.r.t. to the package center (yellow arrows).

2nd level solder joint reliability was investigated by accelerated thermal cycling tests at ¬40/125°C. In the upper part of figure 1 cross-section images of Radar die after cycling on board are shown. The typically evolved fatigue modes, Under-Bump-Metallization (UBM)-, RDL- and solder-ball fatigue, due to the release of thermo-mechanical stress, are presented. Furthermore, to investigate these fatigue modes across the entire package (in 3 dimensions) additional methods of examination, as Scanning Acoustic Microscopy (SAM) and a new analytic technique of chemical "delayering" was used (figure 1 lower part). The orientation of the fatigue modes is indicated by yellow arrows and radially from the edge of the package to the center.

A continuous improvement of the eWLB technology is necessary, due to changing customer requirements, e.g. the modification of the layer structure or stiffness of the PCB, changing sizes of the package and Si, or the demand of higher number of temperature cycles on board [13] [14]. The improvement of the 2nd level solder joint reliability of our devices can be realized by several methods, summarized in figure 2. Additionally, the impact of the presented method is compared to a standard device/condition.

The main positive effects on 2nd level solder joint reliability will be achieved by the introduction of an underfill or cornerbond, adding redundant balls and increasing the size or changing the alloy composition of the solder-balls. Additionally, reducing the temperature difference (Δmin/max temperature) during the cycling process or decreasing the package thickness also improves the number of cycles.

On the other hand, there are various parameters which decrease the 2nd level solder joint reliability. For example, choosing a stiff RF laminate used with the multilayer PCB [21] [22], using no UBM or having a housed PCB/die assembly (costumer condition for application) will strongly reduce the cycle number. Also solder mask defined (SMD) pads lead to a lower cycle number in comparison to non-solder mask defined (NSMD) pads.

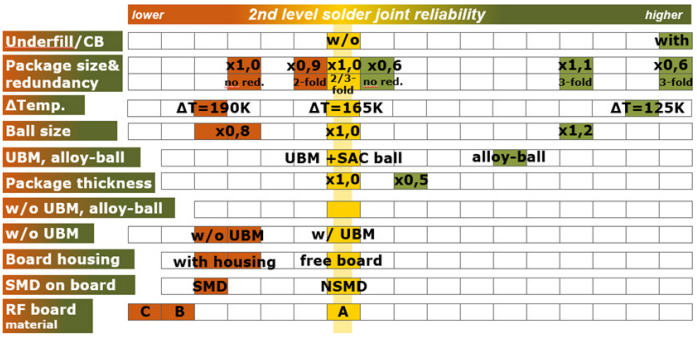

Figure 2: Overview of typical parameters influencing 2nd level solder joint reliability. The colors represent the improvement (green) or degradation (red) of the cycling numbers in comparison to a standard condition/device (yellow).

For analyzing UBM fatigue, the loading at the circular liner interface is investigated using thermo-mechanical finite element simulation. Since Hutchinson and Sou [15] deduced that the interface toughness is much lower for tensile normal loading then for shear loading, the focus is on normal loading. The temperature range from T = -40°C to 125°C was investigated in the simulation. The highest tensile normal loading is present at low temperature (T = -40°C). This can be explained by the reduced creep of the solder ball material at low temperature [16], which leads to a higher elastic stress. Furthermore, at low temperatures a tilt of the solder balls is detectable. The tilt is caused by the mismatch of the CTE's of the PCB and package. As a consequence, the tensile normal stresses are located at the side of the interface oriented towards the perimeter of the package (see figure 3). The color scale in figure 3 visualizes the qualitative distribution of the tensile and compressive stress. These findings from simulation correlates with experimental results from delayering (see figure 1): delamination is also found at the same outer area of the pads.

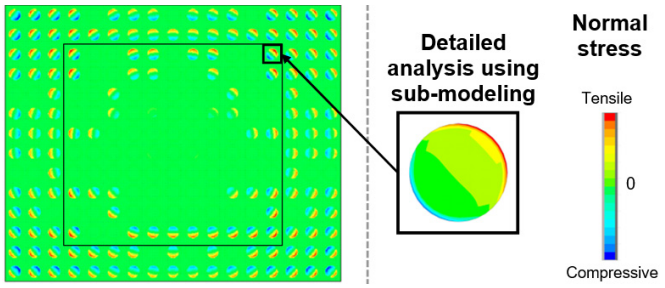

Figure 3: View of the UBM normal stress loading at T = -40°C. The view of a cross-section through the full package (left) shows tensile stresses oriented towards the perimeter of the package. A detailed analysis directly at the liner interface using sub-modeling (right) confirms the distribution. No absolute values are given for the color scales since those vary w.r.t. eWLB package and PCB type investigated.

For understanding RDL fatigue, the complete RDL layer is included in the simulation model and the 1st principal stress in the bulk copper is investigated. The same temperature range as for the UBM simulation was analyzed. As seen with the UBM fatigue, the highest RDL stress loading occurs at low temperature and at the sides of the Cu pads oriented towards the perimeter of the package (see figure 4). Additionally, the indication of higher stress loading for wider Cu-RDL connections was found. This finding correlates with experimental results of the delayered dies in figure 1.

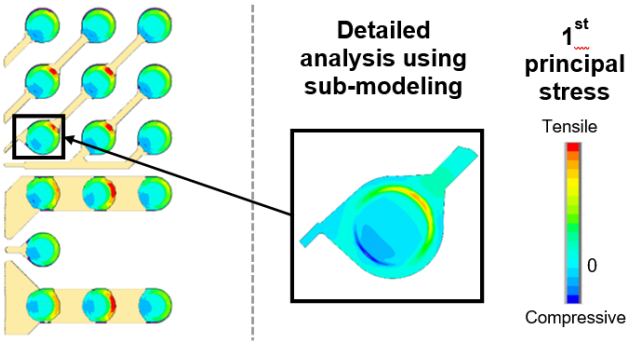

Figure 4: RDL stress loading. Left: View of the 1st principal stress in the RDL layer for a part of the package at T = -40°C. Tensile stresses (red color) are located at the side of the oriented towards the perimeter of the package. Right: Close-up view of single tear drop analyzed in more detail using sub-modeling. No absolute values are given for the color scales since those vary w.r.t. eWLB package and PCB type investigated.

Solder fatigue is analyzed using the framework suggested by Darveaux [17] and Syed [18]. The increment in accumulated in-elastic strain as well as the increment in accumulated in-elastic strain energy density at the solder ball is calculated during temperature cycling [16], [19], [20]. This describes the amount of in-elastic energy put into the solder material per cycle. In the following, the in-elastic energy dissipated per cycle is referred to "damage parameter". The higher the damage parameter, the earlier the solder balls will fail. The map in figure 5 shows the distribution of the damage parameter across the solder balls of the package:

- The damage is high at the balls located at the package corner (red color). This is because the corners have the maximum distance to the package center and, hence, have the highest thermal strain mismatch.
- The damage is high (red color) below the perimeter of the silicon chip and especially at the chip corners. The silicon chip is stiffer than the molding compound and has a lower CTE. This is the reason for the high damage loading similar to the level near the package corners.

In general, this finding agrees with results from cross-sections of devices after solder joint reliability experiments, e.g. as partially shown in [21].

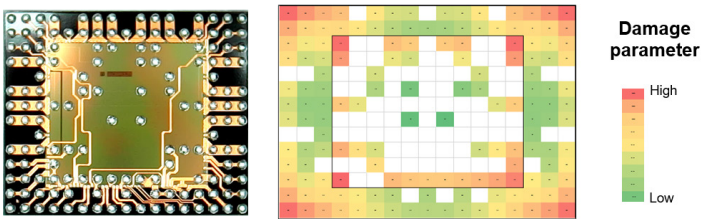

Figure 5: Map of the distribution of the damage loading on the solder balls across the package. Red color indicates high damage, green color indicates low damage. No absolute values are given for the color scales since those vary w.r.t. eWLB package and PCB type investigated as well as the material model used for the solder.

To evaluate whether a respective fatigue mode is able to cause end-of-life, that means an electrical open of the device, the "driving force" of each fatigue mode is analyzed as listed in table 1.

Table 1: Fatigue modes and their driving force.

Fatigue mode	Driving force	Type of fatigue
UBM fatigue	Tensile normal force at interface F_T	De-bonded/opened UBM interface area
RDL fatigue	Tensile 1st principal stress σ_1	Length of cracks in pad of RDL
Solder fatigue	Damage parameter W_i	Cracked volume/ area at solder ball

The magnitude of all three driving forces depends on the geometry and the material parameters of the assembly. The simulation is used to analyze the changed input of driving force in the whole system with increasing level of the respective fatigue type. Figure 6 shows qualitatively two potential outcomes of this analysis: Either the driving force gets lower with increasing level of fatigue, allowing to stop the fatigue mode or the driving force does not reduce, thus allowing to reach a fatigue level of 100%, eventually causing end-of-life.

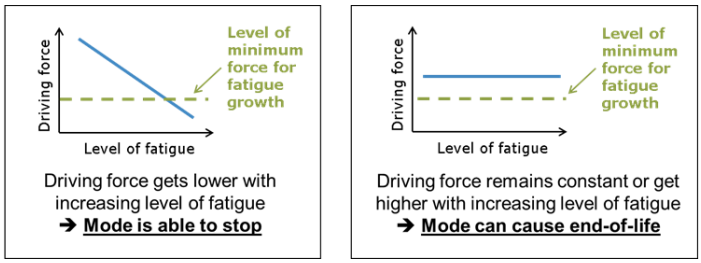

Figure 6: Potential outcomes of the analysis of driving force vs. level of fatigue. Depending on how the driving force evolves with increasing level of fatigue, the mode may either be able to cause end-of-life or not.

To this purpose, detailed sub-modeling of a single ball at a selected location of package is done and combined with a script, which subsequently changes the respective fatigue level. Separate simulations are done for each fatigue mode. The results show that the driving forces of both UBM fatigue and RDL fatigue reduce

with increasing level of fatigue (see figure 7). This is because the assembly of package and ball gets more compliant with increased level of fatigue, i.e. with more debonded UBM area or longer crack in the RDL pad, thus reducing the force for further driving the fatigue. The reduced forces may eventually no longer be able to drive the UBM and RDL fatigue modes when dropping below the critical values needed to propagate the fatigue. Consequently, neither the UBM nor the RDL fatigue mode may cause an end-of-life of the assembly for the investigated loading.

The solder fatigue mode shows a different behavior: The driving force, represented here by the damage parameter wI (here: in-elastic strain energy density) multiplied with the remaining volume VR of the layer of solder ball at the package side, thus constituting the in-elastic energy dissipated per cycle, does not reduce with increasing fatigue level, but remains constant and/or slightly increases. The interpretation is, even for severe solder crack level, e.g. 50% or 80%, this fatigue mode will not stop, but further propagate the crack. Hence, solder fatigue will eventually cause an end-of-life of the assembly.

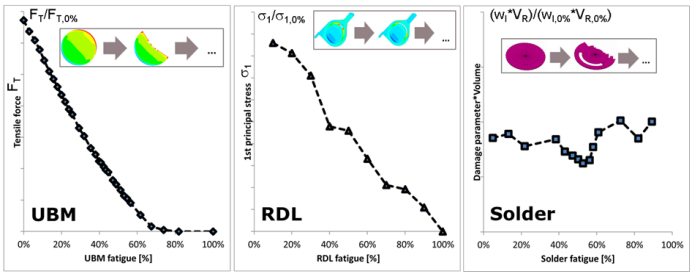

Figure 7: Plots of the driving force of each mode in the simulated assembly versus its fatigue level. Only one fatigue mode is considered in each simulation. Comparing to Figure 6, both UBM and RDL fatigue show behaviors indicating that these fatigue modes will not cause end-of-life, whereas solder fatigue is able to cause end-of-life.

II. RF-PERFORMANCE

EM simulation is used to optimize the chip-package-board transitions, to increase system efficiency or to evaluate different used cases, which cannot be produced or measured easily. The last one is the case for evaluating the RF performance for different fatigue levels as described above. As demonstrated by Seler [23], EM simulation coincide very well with measurements, which is fundamental for chip-package-board co-design.

RF characterization and optimization are performed using ANSYS HFSS full-wave EM simulator that solves the full system of Maxwell equations. RF performance of transitions is evaluated using scattering parameters (S-parameters). The S-parameter matrix is a frequency-dependent matrix that relates reflected and transmitted EM waves. This description considers all EM phenomena's and interactions inside the simulated 3D structure. In particular, return loss on board and chip side (S11, S22) and insertion loss (S21) are important parameters, which need to be characterized and optimized.

In the following part, the influence of the RDL-, UBM- and solder ball fatigue modes on RF performance is evaluated.

Simulation results show that all fatigue modes have negligibly impact on levels of return and insertion loss independently from the fatigue mode and their extent. However, due to a different surface current distribution in case of fatigue modes, the electrical length of the transitions may slightly change. In figure 8 the surface current distribution is shown for two RF transitions. On the left side without any fatigue and on the right side with RDL, UBM and solder ball fatigue.

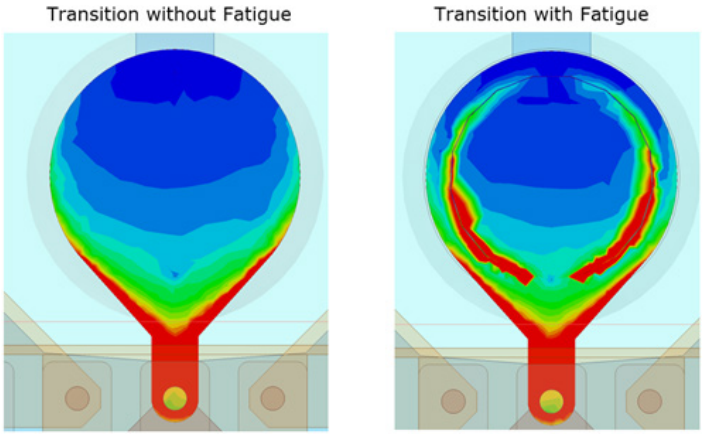

Figure 8: Comparison in surface current distribution of electrical pads with and without fatigue mode. Left picture without any fatigue: Current is concentrated mainly in the narrow RDL area close to the die (red/yellow); Right picture with RDL/UBM/solder ball fatigue: Current is forced to distribute on a wider area on the RDL pad.

Surface current density is lower in the blue regions and higher in the yellow and red areas. This slightly different electrical length will cause difference in phase Φ(S21) of the insertion loss which is undesired in radar applications. It is therefore important to demonstrate that none of the fatigue modes and their combinations lead to phase shift exceeding a specified limit.

In figure 9 the effects of each single fatigue mode (RDL-, UBM- and solder ball fatigue) and two further combinations of them are summarized. The phase shift ΔΦ(S21) is evaluated considering as reference an RF transition without fatigue. For fatigue levels up to 90% the phase shift stays within specification (white area) considering RDL-, UBM- and solder ball fatigue separately. Even the combination of up to 90% of RDL- plus 90% of UBM fatigue indicate acceptable phase shift. Only for an unlikely mix of all three modes with 90% fatigue (RDL-, UBM- and solder ball fatigue), the phase shift may exceed the specification limit (gray area). More than 90% fatigue (e.g. 100%) does not need to be considered, since 100% will cause an electrical DC open. Reliability tests for electrical DC open is done by typical 2nd level solder joint investigations with a standard daisy chain concept.

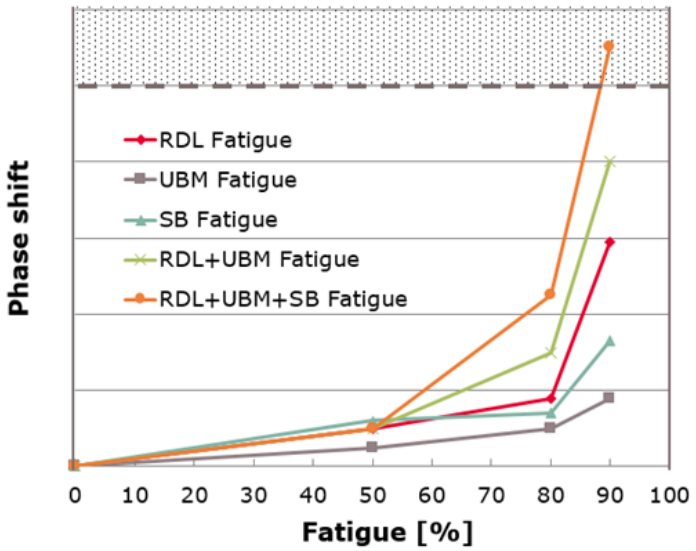

Figure 9: Results for the simulated phase shift depending on the fatigue modes (RDL-, UBM- and solder ball fatigue) and combinations (RDL + UBM-fatigue, RDL + UBM + solder-ball-fatigue).

The RF ports are not located at thermo-mechanically critical positions like package or die corners and therefore have significantly less than 90% fatigue. This is why the phase shift caused by fatigue is expected to be less than the specified limit.

III. THERMAL-PERFORMANCE

Typical power consumptions for automotive MMICs are in the range of P = 1-3W. To remove the heat associated with this power consumption the thermal resistance of the MMICs must be sufficiently low in order not to exceed typical thermal boundary conditions (e.g. T = 85°C for the sensor ambient temperature and T = 125°C for the Si chip bulk temperature). Therefore, the heat must be conducted via the solder balls to the metal layers on the PCB, which are connected thermally to the sensor housing.

To improve heat dissipation, so-called thermal balls have been implemented in the MMIC design. These thermal balls are located in areas of the Si chip, which are not critical for the RF functionality. More thermal balls are desired for improved heat dissipation. However, max. number of thermal balls is an optimum for required thermal and RF performance versus the cost of the Si area. Also, to achieve a low thermal resistance from the balls to the Si chip, metal as much as possible is used in the metallization of the Si in the area of the thermal balls

Thermal simulation shows that the thermal balls on the silicon chip area are very effective and conduct almost 70% of the generated heat. Balls located on the fan-out area of the package are not very effective in lateral heat transfer due to the long distance from the silicon chip to the solder balls and the limited thickness of the Cu RDL redistribution layer (figure 10).

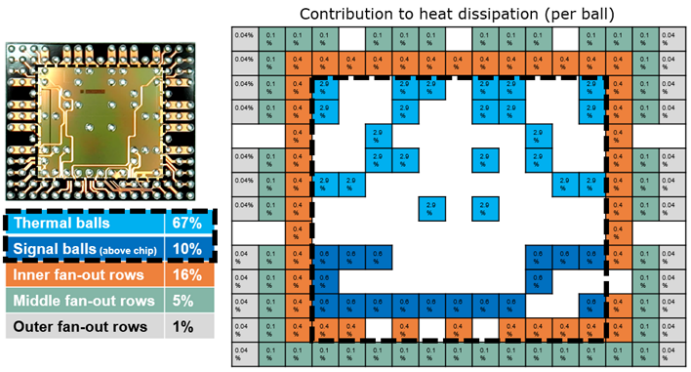

Figure 10: Image of an eWLB Radar die and a schematic illustration of the contribution of each solder ball to the overall heat dissipation for a typical eWLB Radar package. The table represents the sum of the proportion of each ball group.

"How do thermal measurements fit to thermal simulations, and how does the thermal behavior change over lifetime of the package?"

Temperature driven fatigue modes as described above, are leading to a loss in contact area and in consequence to an increase of temperature and Rth. An assessment of that fatigue behavior on thermal performance is done by simulation. Thermal simulation and optimization are done via steady state thermal simulations with ANSYS V19.1 software tool.

The thermal performance or response for different use cases is plotted in figure 11. The corresponding use cases with different degradation or fatigue levels of the balls are shown in figure 12. Assuming 50% degradation in average for all thermal balls, an increase in Rth of up to about 30% is seen. However, not all thermal balls are located at thermo-mechanically critical positions like the die edge. Therefore, Rth change will be typically less than 30%.

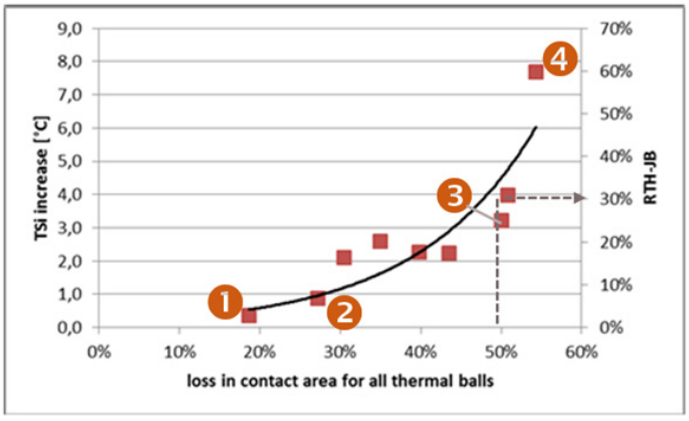

Figure 11: Thermal simulation results for various use cases as shown in figure 12 for a power consumption of about P = 3.3W.

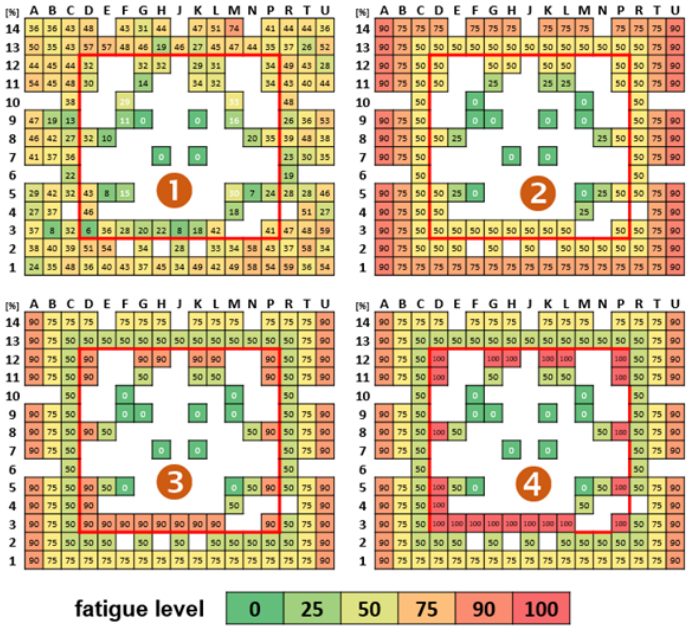

Figure 12: Various use cases 1-4 with different fatigue levels of the balls for assessment of the thermal behavior of the package.

CONCLUSION

Typical fatigue modes of 2nd level solder joints after thermal cycling on board are solder ball-, UBM- and RDL-fatigue. Standard and new analysis methods reveal that all fatigue modes are orientated radially from the edge of the package to the center. Typical measures to improve 2nd level solder joint reliability for the eWLB technology are listed and rated. The UBM-, RDL- and solder fatigue modes are analyzed using thermo-mechanical finite element simulation. The results show that the input of the driving forces in the system of both, UBM- and RDL-fatigue reduce with increasing level of fatigue and do not cause an end-of-life failure. For solder fatigue, the driving force does not reduce, but remains constant and eventually causes an end-of-life failure.

For evaluating the fatigue modes on the RF performance, the phase shift on the RF transmission Φ(S21) is analyzed. For fatigue levels up to 90% the phase shift stays within the specified limit considering RDL-, UBM- and solder ball fatigue separately.

Thermal simulation shows that the thermal balls on the silicon chip area are very effective and dissipate almost 70% of the generated heat. For assessing several different use cases with different level of fatigue for each ball positions across the package ball out, thermal simulation shows that e.g. assuming 50% degradation in average for all thermal balls, an increase in Rth of up to about 30% is seen.

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BIOGRAPHIES

Walter Hartner received his M.Sc. degree in Physics from the Friedrich-Alexander University of Erlangen, Germany in 1995 and his Ph.D. from the Technical University of Aachen in 2003. He joined Siemens AG in 1995, where he first was engaged in process development and integration for ferroelectric memory in Munich, Germany and Colorado Springs, USA, and later for 110nm DRAM for Infineon Technologies in Richmond, Virginia USA. Since 2003, he is with Infineon in Regensburg, Germany. After innovating the Deep Trench Isolation concept incl. an integrated substrate contact for new generations of Smart Power Technologies, his primary development interests since 2009 are in embedded wafer level package technologies (eWLB). As project manager and as lead principal engineer, he is responsible for automotive radar package applications. He has authored and co-authored more than 40 articles and he holds more than 60 patents in the field of semiconductor frontend and backend technology.

Martin Niessner is principal engineer at Infineon Technologies. He received his Ph.D. in electrical engineering with first class honors from the Technical University of Munich (TUM), Germany. From 2006 to 2012, he was a researcher and teaching assistant with the MEMS group of Prof. Dr. habil. G. Schrag and Prof. G. Wachutka at TUM, focusing on the systematic characterization and physics-based multi-energy-domain coupled simulation of MEMS devices. Since 2012, he is with the package simulation team at Infineon Technologies AG, Neubiberg, Germany. His work focuses on reliability prediction, material characterization, material modeling and standardization (JEDEC/IPC-9301 guideline) in the field of microelectronics packaging.

Francesca Arcioni studied at the University of Pavia, Italy, where she received her master degree in electronic engineering. She joined Infineon Technologies AG, Munich Germany in 2000 and the EM simulation department in 2007. She is a Principal Engineer for electrical simulation and she has been working on several package technologies for different applications and different frequency ranges. Since 2015 her primary focus is on electromagnetic simulations for radio-frequency and mm-Wave, supporting product development for automotive radar applications in wafer-level package technology.

Markus Fink is a staff engineer for simulation at Infineon Technologies AG. His experience ranges from thermal package simulation for almost all package platforms at Infineon, thermo-mechanical FE analysis and material modeling. During his 20 years at Infineon he supported several projects for package development and managed different programs for developing new simulation methods. He holds a Master degree in micro systems technology from the University of Applied Sciences in Regensburg, Germany

Christian Geissler is packaging innovation engineer in the sensor backend technology innovation group at Infineon Technologies in Regensburg, Germany. He received his M.Sc. degree in Physics from the University of Regensburg in 1997 and joined Siemens/ Infineon in 1997. He worked as device expert and project manager on different frontend and backend technology development projects until he joined Intel in 2011. Together with external partners, he focused on reliability improvements and platform extension of wafer level and panel level packaging technologies. In 2015 he returned to Infineon Technologies and took over the technical lead of sensor packaging projects in various packaging platforms and participates in several national and international funding projects.

Gerhard Haubner is currently working as Principal Engineer for Reliability Engineering at Infineon Technologies in Regensburg/Germany. After positions at package development with emphasis of the transition to lead-free soldering he joined over 15 years ago the corporate department for package reliability. His main focus is advanced packaging, especially wafer level packaging, where he performs lifetime determination and develops lifetime models. Particularly the 2nd level interconnect reliability is part of his work. Gerhard is also actively participating in several standardization development organizations like JEDEC, IPC and IEC in order to harmonize quality and reliability concerning packaging standards.

Maciej Wojnowski is the Lead Principal Engineer and the Head of RF Package Simulation & Characterization in the central development department at Infineon Technologies AG. He has been with Infineon Technologies AG, Munich, Germany, since 2005. He has been working in development of RF and millimeter-wave passives and antennas for system-in-package applications. He was responsible for electrical characterization of the embedded Wafer Level Ball Grid Array (eWLB) technology. He is the author or co-author of more than 50 papers and 30 patents in the areas of RF and millimeter-wave packaging and passive device characterization. Dr. Wojnowski is recipient of the 2018 IEEE Outstanding Young Engineer Award "For Leadership and Contributions to the Fields of Millimeter-Wave Packaging and Passive Device Characterization". He serves on the Technical Committees of the IEEE MTT-16 and the ECTC conference and as reviewer for several journals and conferences.