Board Level Reliability of Automotive Grade WLCSP for Radar Applications

Nishant Lakhera, Burt Carpenter, Trung Duong, Mollie Benson and Andrew J Mawer
NXP Semiconductors
Austin, Texas, USA

ABSTRACT

Wafer-Level Chip Scale Packages (WLCSPs) are becoming commonplace in the industry due to their small form factor. Applications include industrial and automotive which demand high reliability performance. Additionally, WLCSPs may be superior in some implementations to other package options for RF performance in the mmWave spectrum, which is desired for automotive radar application. But board level reliability can be a challenge for some WLCSP packages due to CTE mismatch between Si and PCB. A variety of factors including PCB materials, sphere alloys, and board level underfills can influence the board level reliability of WLCSP packages. In this study the industry's first auto grade 1 capable large WLCSP package. (~ 72 mm2 body size, 18x15 BGA array, 0.5 mm pitch) is presented. Board level underfill application was utilized to achieve automotive grade board level reliability. Underfills are typically selected based on thermomechanical properties of unaged materials. An understanding of the evolution of underfill material properties under thermal aging is important for selecting a stable material capable of meeting the reliability requirements.

This study evaluates board level underfills and edge bond materials in the form of stand-alone samples and applied to a large daisy-chain WLCSP. The underfilled daisy-chain WLCSPs and the stand-alone samples are placed in a 40/125C air cycling chamber (1 cycle/hour). Glass transition temperature (Tg), elastic modulus (E), and coefficient of thermal expansion (CTE) are measured using Dynamic Mechanical Analysis (DMA) and Thermomechanical Analysis (TMA) on the stand-alone samples at various intervals to monitor the evolution of material properties. Simultaneously, the underfilled daisy chain WLCSPs are monitored electrically using an event detector. The combination of material property measurements and cycles to electrical failure can be used to correlate underfill material properties and WLCSP board-level reliability. The results of this study can provide material property guidance for underfill selection.

Key words: solder joint reliability, underfill, CSP/chip scale package, edge bond, board level reliability

INTRODUCTION

Electrification, safety and autonomous driving are the megatrends in the automotive industry. The automotive electronics industry is undergoing explosive growth to support these megatrends. Radar sensors in automobiles play a critical role today in advanced driver assistance systems (ADAS) and in future will be instrumental in enhancing autonomy. Demand for more diverse applications and better performance in automotive and industrial electronics is growing astronomically, pushing the industry towards utilizing advanced packaging technologies instead of legacy technologies. The size of electrical components must shrink without sacrificing functionality, which makes Wafer-Level Chip Scale Packages (WLCSPs) an attractive solution for radar applications. However, automotive and industrial applications require high board level reliability performance in severe environments, and WLCSP board level reliability is complex [1]. Automotive packages are typically required to pass at least 1000 cycles of board level temperature cycling. Board level reliability can be improved using a variety of solutions, including lower CTE printed circuit board (PCB) core materials, fatigue resistant sphere alloys, board level stiffening materials like edge bond, and underfills. However, often the most desirable options for manufacturing ease and cost purposes are underfill and edge bond [2, 3, 6, 7]. Underfills and edge bonds selection is based on key material properties, primarily the coefficient of thermal expansion (CTE), the glass transition temperature (Tg), and the modulus (E) [4]. The material properties reported in supplier datasheets are usually measured at time zero conditions after the material is fully cured, but properties can change as a function of environmental stress during reliability stressing. Therefore, selecting underfills and edge bonds based on published datasheet values of CTE, Tg, and E may not yield the best reliability. Monitoring the evolution of these material properties under high stress thermal conditions can provide insight on how a material changes in response to its environment. Understanding this mechanism is critical for the underfill selection process, and can

help determine if changes in the material properties correlate with the lifetime of an underfilled WLCSP component. Additionally, it can be determined whether or not CTE, Tg, and E may be the ideal properties for optimizing board level reliability.

This study evaluates both underfills and edge bonds in the form of individual bulk material samples and applied to a large daisy chain WLCSP. Both the samples and the underfilled/edge-bonded components are thermo-mechanically stressed, with the daisy chain components being monitored electrically and the individual samples being removed from cycling at predetermined intervals for material property measurements. A detailed design of experiment, testing protocol, and results are described below.

EXPERIMENTAL

Detailed experiments were designed to investigate factors influencing board level reliability performance of large WLCSP package, as described in sections below.

Test Vehicle for Board Level Thermal Cycling

Daisy chain (DC) test vehicles were used in the evaluation to continuously monitor the solder joint integrity during thermal cycling testing. The goal of the test vehicle (TV) was to emulate the product as closely as possible from design perspective. A custom die with 7.9 mm x 9.3 mm body size, 18 x 15 solder ball grid array (BGA) array, 0.5 mm pitch was fabricated with daisy chain in the last metal of the silicon to monitor the integrity of the silicon backend during thermal cycle testing. Standard SAC alloy was used for this study. WLCSP redistribution (RDL) layers were modified to form daisy-chain nets to include silicon last metal, bond to RDL interface, RDL to under bump metallurgy (UBM) interface, UBM to BGA interface, BGA to PCB pad interface and the PCB traces. Example schematic is shown in Figure 1 and actual daisy chain TV is shown in Figure 2.

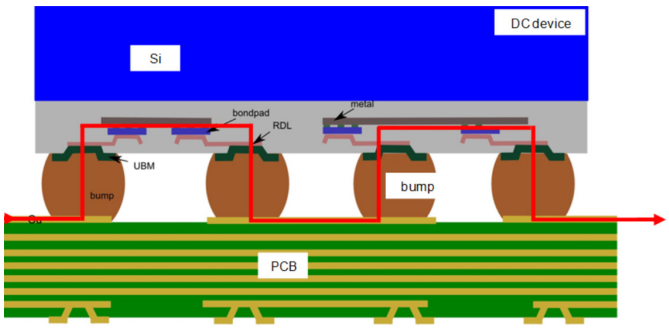

Figure 1. Daisy chain test vehicle schematic

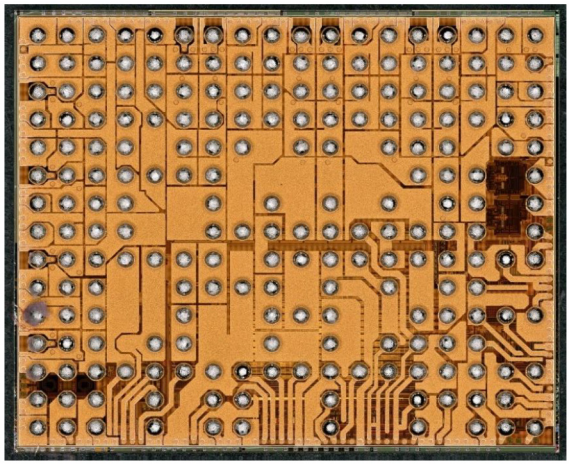

Figure 2. Daisy chain TV bottom view

PCB and Board Assembly Process

The corresponding PCB had a complimentary DC that completes the electrical path when TV was assembled on the board. All of the cells of this DOE were assembled using a non-soldermask defined (NSMD) PCB pad, as shown in Figure 3. The PCB used for this evaluation had 4 copper layers and a high-Tg FR4 core.

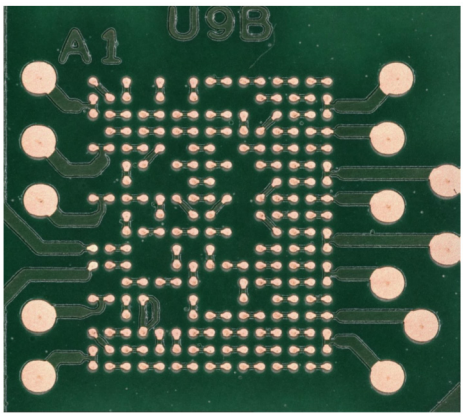

Figure 3. NSMD PCB pads used for this study

Prior to assembly, the DC components were baked at 125C for a minimum of four hours to remove any moisture. No- clean solder paste was applied to the PCB, and the printed PCB was inspected optically for print accuracy and uniformity. Once the PCB passed visual inspection, components are assembled on the board. The fully populated PCB underwent reflow in air, and once cooled it was electrically verified with an ohmmeter. The assembled PCB was also visually inspected using x-ray to verify no solder paste bridging and good solder joint formation, as shown in Figure 4. Only PCBs that passed 100% inspection were used for this evaluation.

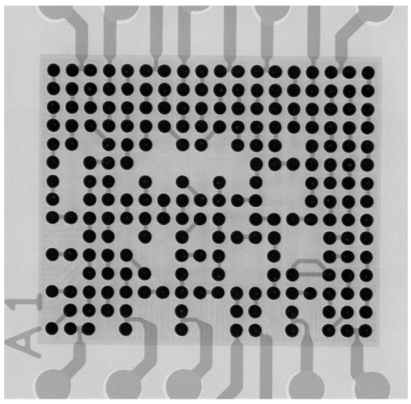

Figure 4. XRAY images of assembled DC TV on PCB

Underfill Materials

Five board level materials were evaluated, including three capillary underfills and two edge bonds. These materials were selected based on following material properties: low CTE, high Tg, and low room temperature modulus. The nomenclature and supplier published values for the aforementioned material properties are listed in Table 1. NXP measured CTE-1 and room temperature modulus is also shown for comparison.

Table I. Underfill and edge bond nomenclature and material properties.

Cell	CTE-1 (ppm/C)	Tg (C)	E (GPa)	CTE-1 NXP TMA (ppm/C)	E 25C NXP DMA (GPa)
UF1	32	135	8.0	31	10
UF2	27	135	12.0	24	15
UF3	30	130	6.7	35	9
EB1	15	149	13.3	19	18
EB2	30	134	7.6	36	9

Each cell is evaluated using both assembled DC components (16 in total) and bulk underfill and edge bond samples prepared for material property testing. Both the assembled components and the bulk samples were subjected to board level reliability cycling conditions of -40/125C.

Sample Preparation

All of the underfills were applied to the assembled PCBs using an Asymtek M-620 Platform with a DP-3000 Positive Displacement Pump. The optimized curing profile for each underfill was provided by the underfill suppliers and was followed for this evaluation. An example of an underfilled component can be seen in Figure 5a. All edge bond application was performed externally due to internal lab limitations, and the curing profiles for both edge bonds were prescribed by the edge bond suppliers. The edge bond was also applied in the supplier-recommended pattern, which was a long "L" shape; this can be seen in Figure 5b.

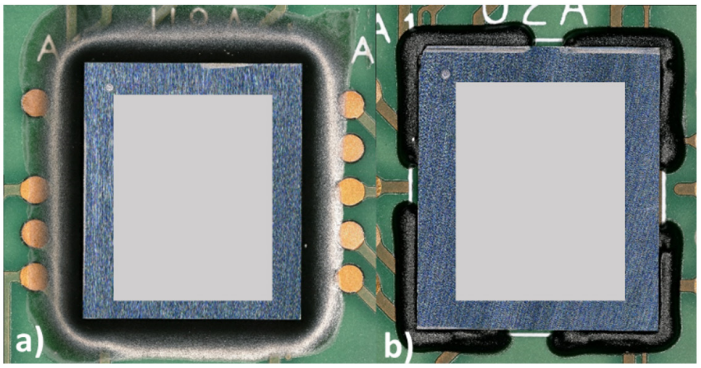

Figure 5. a) Typical underfill application for WLCSP component; b) Supplier-recommended edge bond application pattern for WLCSP component. Proprietary component markings are concealed.

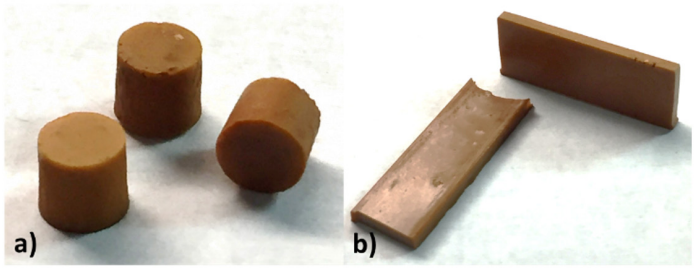

Figure 6. a) Typical TMA sample used for this evaluation. 4.82 mm diameter and 4.45 mm height; b) Typical DMA sample used for this evaluation. Dimensions are 26.75 mm x 2.00 mm x 9.56 mm approximately.

All of the underfilled and edge bonded PCBs were electrically verified once again before entering the cycling chamber. Bulk underfill and edge bond samples were created for material property testing using TMA and DMA analysis as shown in Figure 6.

Thermomechanical Single Chamber Testing

Thermomechanical cycling (TMCL) was performed in a single chamber that cycles from -40C to 125C, with 15 minute ramps, 15 minute dwells, and an 11C/min ramp rate. Each cycle takes one hour, and it takes approximately six weeks to reach 1,000 cycles, as shown in Figure 7.

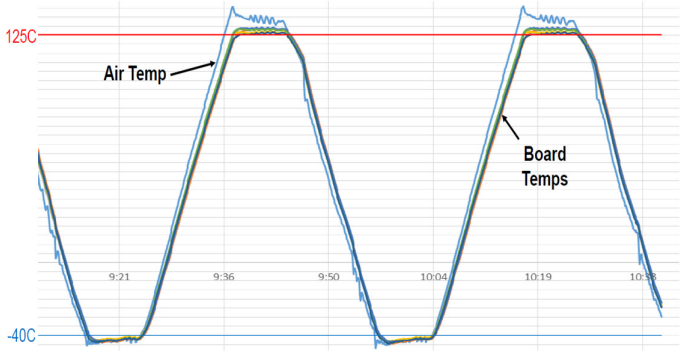

Figure 7. Thermal cycle chamber profiled to achieve prescribed temperatures on board and DC parts

All of the underfilled and edge bonded PCBs that passed electrical inspection were placed into the chamber, and were electrically monitored using event detectors. The cycles to first electrical failure for each component were defined as the first cycle at which the daisy chain resistance increases to 1,000 ohms or greater, followed by nine or more additional events within 10% of the cycles to initial failure [5]. When the first electrical failure occurred for each cell of the DOE, the chamber was stopped and the failure was verified using an ohm-meter. If the failure was real, the failed component was cut out from the PCB and submitted for failure analysis. The remaining PCB was put back into cycling and the chamber was restarted. Only the first failure for each cell was verified, unless FA yielded unusual results. Once the cell reached at least 65% failure, the PCBs from that cell were removed from cycling.

In addition to the PCBs, material property testing samples for each DOE cell were placed in individual metal boxes, as shown in Figure 8. These metal boxes were placed in the chamber, with bulk underfill and edge bond samples being pulled from each DOE cell at 0 cycles, 250 cycles, 500 cycles, 1,000 cycles, and 2,000 cycles to monitor the evolution of material properties of underfill and edgebond.

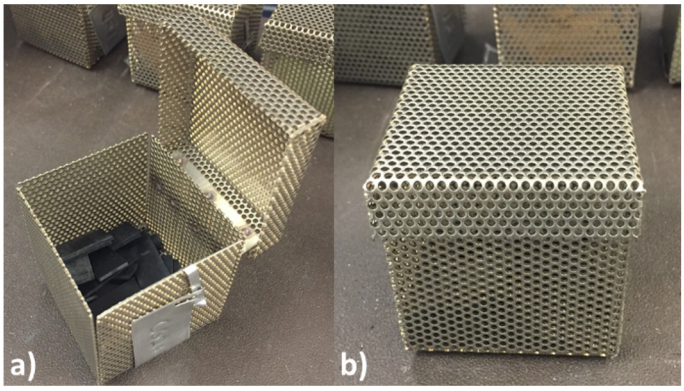

Figure 8. Bulk underfill and edge bond material samples submitted to thermal cycling, a) open meshed container ; b) closed meshed container.

Material Properties Testing

Dynamic mechanical analysis (DMA) testing was performed on the cured underfill test samples to determine the E and Tg using TA Instruments DMA Q800. Testing was performed in 3-point mode with 20 mm span at 1 Hz frequency. A temperature range of -60C to +260C was chosen with a ramp rate of 3C/min. Tg was defined as the peak of the tan delta curve from the DMA. Thermomechanical analysis (TMA) testing was performed on cured underfill test samples to determine the CTE using TA Instruments TMA Q400. A temperature range of -60C to +260C was chosen with a ramp rate of 5C/min. CTE was calculated in the board level thermal cycling temperature range of -40C to +125C. Three DMA and TMA tests per read point were performed to ensure repeatability for the time zero and thermal cycle conditioned samples. Data from DMA and TMA is being reported as the average and one standard deviation from three tests.

RESULTS AND DISCUSSION

Evolution of Coefficient of Thermal Expansion

The evolution of CTE over 2,000 cycles at the aforementioned condition (-40/125C) for all five materials can be seen in Figure 9. Overall the materials did not show any significant change in the CTE as a function of reliability stresses demonstrating the stability of these underfills and edge bond materials under aging conditions. Only a minor reduction in CTE was observed for all materials tested which may be due to additional polymer crosslinking that occurred during thermal exposure. EB2 had highest zero hour CTE while EB1 had the lowest.

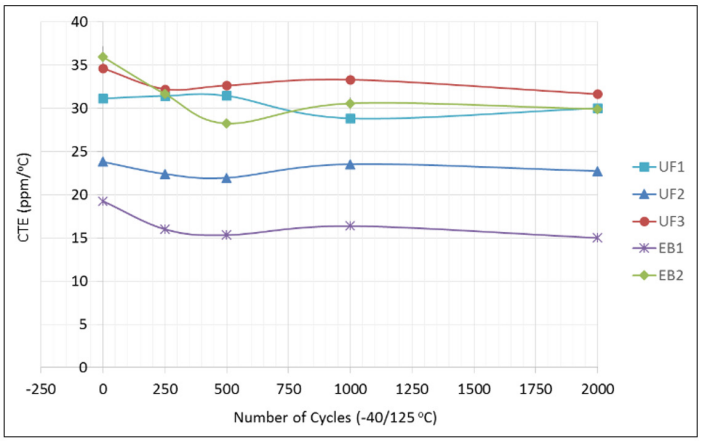

Figure 9. Measured CTE values (calculated via TMA) for each material as a function of TMCL. CTE measured at 0, 250, 500, 1000, and 2000 cycles.

Evolution of Glass Transition Temperature

As seen in Figure 10, the behavior of Tg over 2,000 cycles was generally similar between the five materials. The Tg gently increased and then plateaued, which is to be expected when the maximum temperature reached during cycling is below the Tg of each of the five materials. All of the materials except for UF2 displayed an increase in Tg after 2,000 cycles. The increase in the Tg observed is possibly due to additional polymer crosslinking or physical aging where the polymer chains restructure themselves to form a more dense structure, which also resulted in a corresponding decrease in CTE. UF2 possibly achieved complete polymer structure equilibrium during its initial cure schedule. EB1 had highest zero hour Tg while EB2 had the lowest Tg.

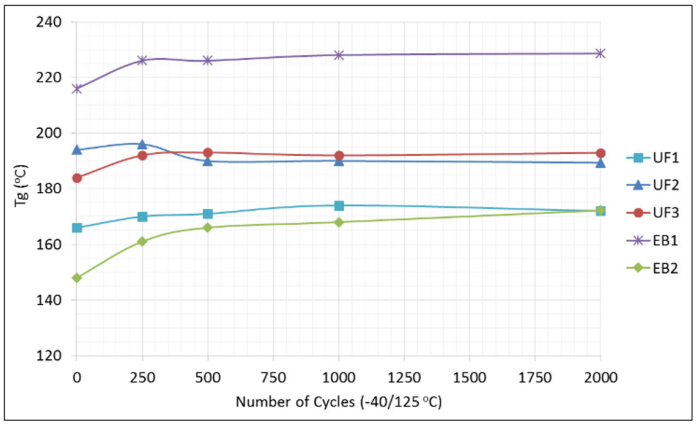

Figure 10. Measured Tg values (calculated via DMA) for each material as a function of TMCL. Tg measured at 0, 250, 500, 1000, and 2000 cycles.

Evolution of Elastic Modulus

Modulus measurements were taken for each material at 40 C, 25C, and 125C to study the material modulus at a range of temperature spanning the thermal cycle condition; the modulus values at each of these temperatures over 2000 cycles can be seen in Figure 11a, 11b, and 11c, respectively. In general, the modulus increased as temperature decreased, which is a typical thermoset polymer material behavior. The materials show a range of elastic modulus due to the different silica filler loading that was used in the formulation. EB1 showed the highest elastic modulus at all temperatures and maintained a fairly stable value over 2000 cycles. UF3 and EB2 showed the lowest elastic modulus at all temperature and did not show any significant change in the modulus as a function of thermal cycling. The stability of the elastic modulus as function of thermal cycle indicates that these materials are fairly stable under the reliability stresses and do not show any material degradation which may have resulted in changes in the material modulus.

Thermal Cycling Results

The relative cycles to failure for all five materials are plotted on a two-parameter Weibull in Figure 12. UF3 resulted in earliest first failure and had lowest characteristic life. UF2 performed the best with highest characteristic life. Cycles to first fail and failure location is summarized in Table II. UF3 had the highest CTE while UF2 had the lowest CTE. As Tg of all materials is well above the thermal cycling temperature range of -40 to 125C therefore, it is concluded to not be a significant factor in the reliability performance of the materials. As thermomechanical stress is a combination of elastic modulus and CTE, a lower CTE and lower modulus material is expected to perform better. All underfill materials investigated in this study were stable during environmental stresses aging condition. Thermal stability of the material is a must during high reliability application but material properties like CTE and modulus are equally important to ensure desired reliability performance is achieved.

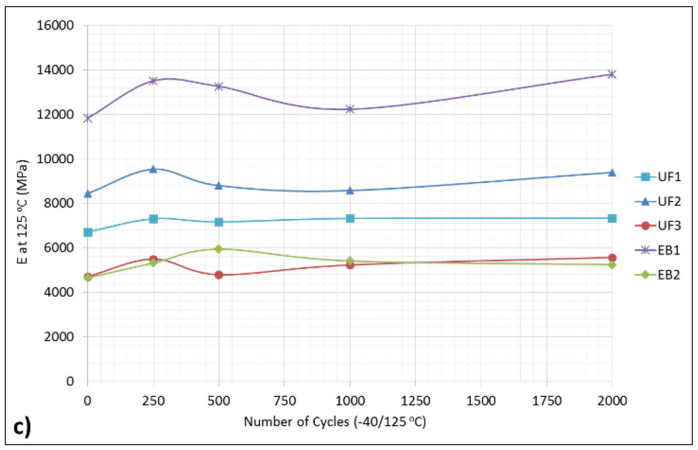

Figure 11. Measured E values for each material (calculated via DMA) at a) -40C ; b) 25C ; and c) at 125C as a function of TMCL. E was measured at 0, 250, 500, 1000, and 2000 cycles.

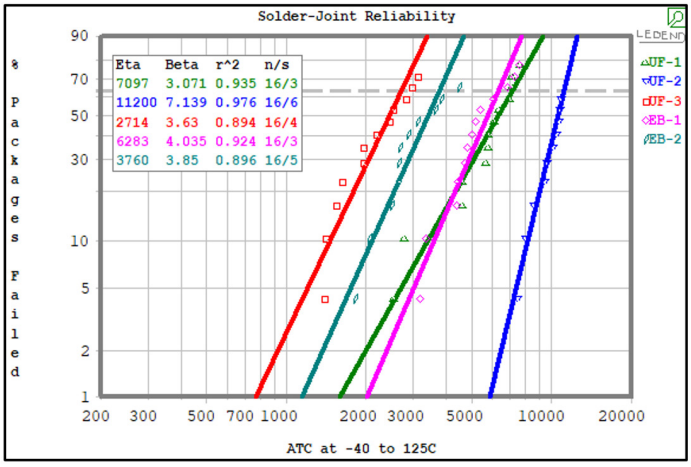

Figure 12. Two parameter Weibull showing board level cycling results

Table II. Board level cycling first fail and failure location

Cell	Cycles to 1st Fail	1st Fail Location
UF1	2547	Not Corner
UF2	7399	Corner
UF3	1388	Not Corner
EB1	3196	Not Corner
EB2	1809	Corner

Failure analysis was performed to assess the failure mode of the first fail observed with UF3. Figure 13a shows live bug view of the device and 13b shows the location of failed solder joint as isolated by curve trace analysis. The failing joint was located in the second row from the bottom in an area with high BGA depopulation.

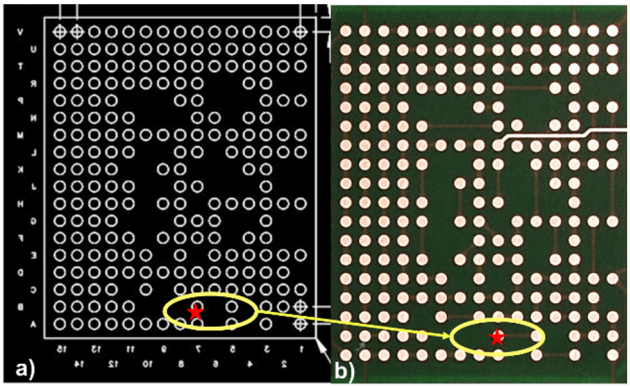

Figure 13. a) Live bug view of BGAs on WLCSP TV ; b) Flat section showing failed BGA for UF3.

Ion-mill cross-section performed on the failed BGA is shown in Figure 14. PCB side crack on the solder joint was observed. This BGA sits on PCB pad with via-in-pad which increases the stress on the BGA ball by reducing its ability to flex during thermal cycling. If the underfill material properties are not optimized for lower solder joint stress, sensitivity to BGA population scheme and PCB design increases resulting in fails in non-corner locations (as observed with UF3 and UF1). UF2 material properties reduces sensitivity to BGA pattern and PCB design and results in classic corner joint failures. Failure analysis was not completed when this paper was compiled.

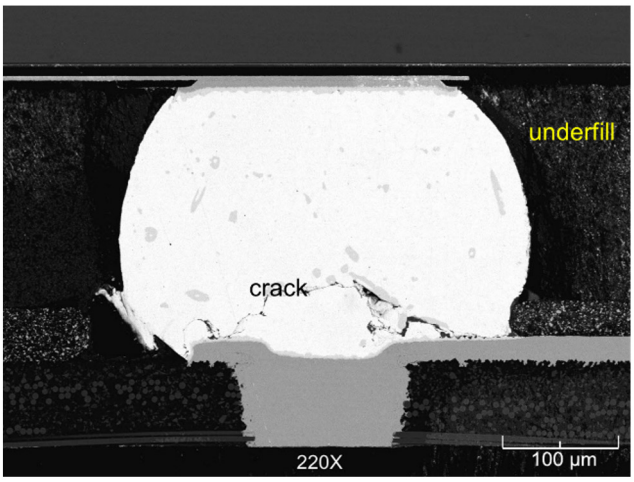

Figure 14. Solder joint cracking on the PCB side for UF3.

Among the edge bond materials EB1 performed 2x better than EB2. Because the dispense patterns were identical for these two materials, the difference in cyclical fatigue performance has been attributed to the material properties. EB2 had significantly higher elastic modulus in the cycling temperature and lower CTE compared to EB1. Edge bond dispense pattern used in this study was L-shape at all four corners. Corner solder joint has highest contact area with the edgebond but is not fully encapsulated, as shown in Figure 15. Edgebond acts as a stiffening agent between the package and PCB and reduces the rocking motion between the package and PCB thereby increasing the solder joint life. Therefore, higher modulus and lower CTE material is preferred to provide higher stiffness to package PCB structure. Larger edgebond volume provides larger contact area between package-PCB-edgebond providing higher stiffness and increased solder joint life. Different edge bond pattern will also influence the solder joint performance and should be optimized for product specific needs.

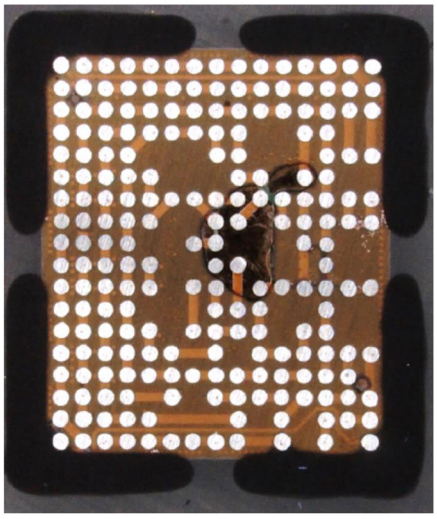

Figure 15. Bottom side flat section view showing edgebond contacting the BGA.

Analysis of first failure performed on edgebond EB1 is shown in Figure 16. Figure 17 shows the ion-mill cross-section of the failing solder joint; crack was confirmed on the package side of the joint.

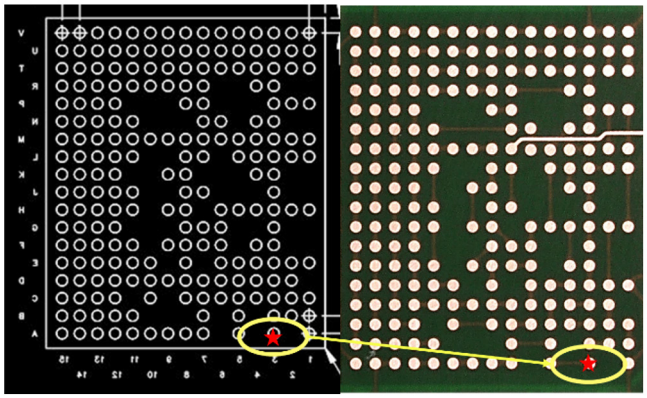

Figure 16. a) Live bug view of BGAs on WLCSP TV ; b) Flat section showing failed BGA for EB1

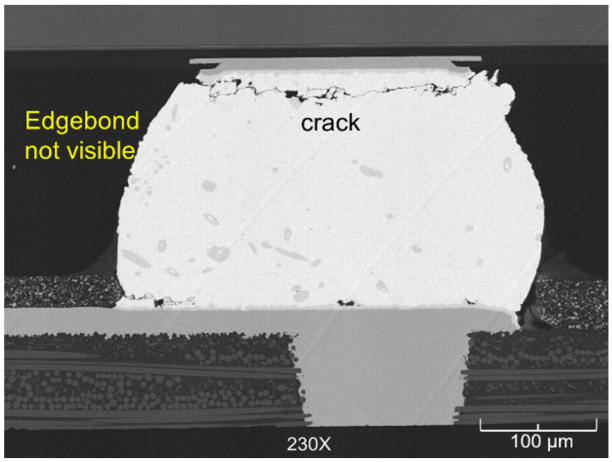

Figure 17. Solder joint cracking on the PCB side for EB1

Board level cycling results were correlated to the material properties of edgebond and underfill and results are shown in Figure 18.

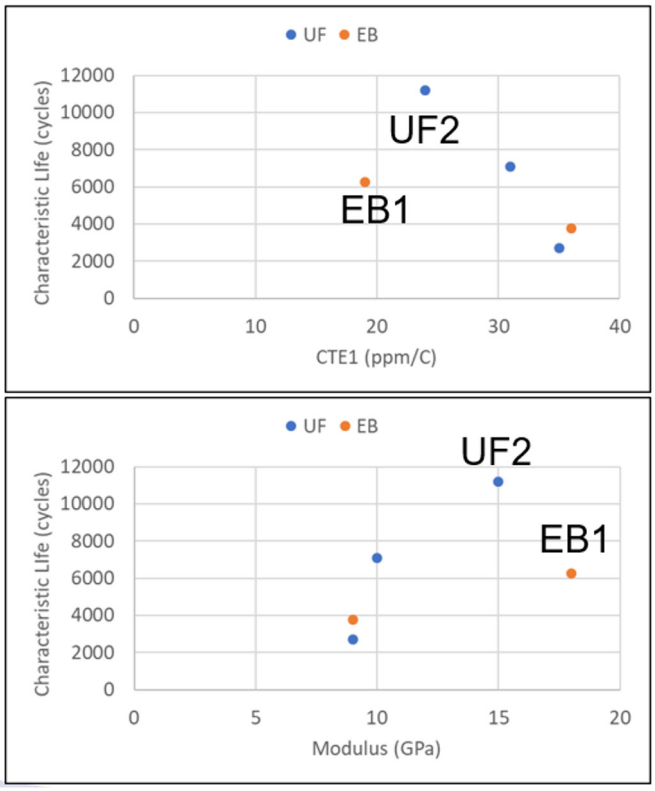

Figure 18. Thermal cycling characteristic life as a function of a) CTE and ; b) Modulus

Amongst the underfill materials, UF2 had the lowest CTE and highest elastic modulus and showed the best thermal cycling performance. Similar material property trend was also observed for edgebond materials with EB1 performed better than UF.

CONCLUSION

This study investigated the impact of thermomechanical properties of underfill and edgebond materials on board level thermal cycle reliability of large WLCSP packages. Thermal stability of board level stiffening materials is imperative to achieve good board level reliability. All materials evaluated in this study did not show any degradation in thermomechanical stability and were able to achieve 1000c before 1st fail. In general underfills are expected to perform better than edge bond materials due to larger material volume as underfill encapsulates all solder balls while edge bond is only dispensed around the edges of the packages. In addition to acting as a stiffening agent underfill material being in direct contact with the solder joint also exert direct thermomechanical stress on it, therefore, optimizing thermomechanical properties is critical for reliability. This study also showed that edge bond materials, if chosen carefully also have the capability to provide good reliability performance to meet automotive requirements. Edgebond acts as a stiffening agent between package and PCB thereby increasing the solder joint life. Edgebond pattern and dispense volume needs to be carefully tuned for application specific needs. Regardless of use of edgebond or underfill materials, key material properties like Tg, CTE and elastic modulus must be carefully designed. Tg above the operating temperature of the product, low CTE and higher elastic modulus can help to optimize solder joint life

ACKNOWLEDGEMENTS

In addition to underfill and edge bond suppliers who generously provided TMA and DMA samples for the purpose of this study, the authors would also like to thank Tara Assi, Paul Galles, Alvin Youngblood, and Les Postlethwait for their contributions to board assembly, underfilling, assembly, failure analysis and Jim Howell for contributions to material property testing.

REFERENCES

[1] P. Nemeth, Z. Illyefalvi-Vitez, and G. Harsanyi, "Review of the reliability of advanced component packaging technologies," in Electronic Components & Technology Conference, Las Vegas, NV, 2000, pp. 1605-1609.

[2] L. Nguyen et al, "High performance underfills development – materials, processes, and reliability," in The First IEEE International Symposium, Norrkoping, 1997, pp. 300-306.

[3] Gyuoyun Tian et al, "Corner bonding of CSPs: processing reliability," IEEE Transactions on Electronics Packaging Manufacturing., vol. 28, no. 3, July 2005, pp. 231-240.

[4] M. C. Paquet, M. Gaynes, E. Duchesne, D. Questad, L. Belanger, and M. Sylvestre, "Underfill selection strategy for Pb-free, low-K and fine pitch organic flip chip applications," in 56th Electronic Components and Technology Conference, San Diego, CA, 2006, pp. 1595-1603.

[5]Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, IPC Standard 9701A, Feb. 2006.

[6] A. Mawer, B. Carpenter, and M. Benson, "Package Technologies for Advanced Automotive Applications", SMTAI 2019, Rosemont, IL

[7] A. Hsiao, TK Lee, E Ibe, and K Loh, "Multi-Axis Loading Effect on Edgebond and Edgefilled WLCSP Thermal Cycling Performance", SMTAI 2019, Rosemont, IL

BIOGRAPHIES

Nishant Lakhera holds a PhD in Mechanical Engineering from University of Wyoming and is currently working at NXP Inc., Austin, TX, USA as a Semiconductor Packaging Engineering Manager where he is responsible for development and implementation of packaging solutions for automotive and non-automotive products. Nishant holds 14 US Patents (11 granted, 3 pending) and has published numerous articles in internal journals and conference proceedings.

Mollie Benson works at NXP Semiconductors in Austin, TX as a Packaging Engineer for Analog and Mixed Signal Packaging. She previously supported the Product Diagnostic Lab for three years, where she managed the Board Level Reliability and Package Analysis activities. Mollie joined NXP in 2017 and has had a variety of packaging experience including Board Level Reliability (Thermal Cycling and Shock, Monotonic Bend, and JEDEC Drop testing), SMT assembly, PCB design, and failure analysis. Mollie has a Bachelor of Science degree in Materials Engineering from California Polytechnic State University, San Luis Obispo.

Andrew Mawer is the Global Package Design Manager at NXP Semiconductors in Austin, TX. Immediately prior to that he managed an analytical and reliability laboratory. Andrew has been with NXP, formerly Motorola then Freescale for a total of 28 years. Andrew previously spent four years at HP where he was involved with the implementation of some of the first high pin count PBGAs in the industry. He has authored and presented over 40 papers and authored two book chapters. He is an active member of SMTA and has served on the Technical Committee of the SMTA-I Conference, the Review Board of the SMTA Journal and with various leadership roles within the Central Texas SMTA chapter. He received the SMTA National Member of Technical Distinction Award in 2007. Andrew received his B.S. in Mechanical Engineering from the University of Texas in 1987 and M.S. in Mechanical Engineering from Rice University in 1989. He received the Outstanding Young Mechanical Engineer Award from UT's Mechanical Engineering Dept in 2007.