Freeze Frame Reflow to Enhance Yields for Advanced Low-Profile Bottom Terminated Packages

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ABSTRACT

Today, designers are demanding an overall form-factor reduction to save board space, increase functionality, and allocate more circuit board real estate toward end-user applications – all with less space allocated to power management where not just the X-Y shrink but the 3D volumetric shrink is required. Unlike most gull wing style leaded packages, QFNs (Quad Flat Pack No lead packages) also known as BTCs (Bottom Terminated Components) have coplanar terminals below the package body to answer this ever-decreasing form-factor requirement. The final standoff in these QFN style packages are dictated by the solder joint geometry formed. Within this advanced package family also finding a similar trend are power WCSPs (Wafer Chip Scale Packages) where traditional solder spheres are being replaced with low profile interconnects in expanded and asymmetrical geometries.

This paper presents factors that influence advanced low standoff package solderability performance with the use of video microscopy and live in situ X-ray reflow. To reflect the QFN board assemblies that are typically designed a series of layouts were implemented across different coupon test boards. Assembled coupon test board were designed by varying 1) through hole via design, 2) solder mask tenting techniques, 3) periphery and center thermal pad printed solder joint volumes, 4) no-clean and water-soluble solder paste flux chemistry all using SAC 305 alloy and type 4.5 powder size. One case study using live in-situ X-ray system will explain the effects of a QFN land pattern layout incorporating vias in the center thermal pad with solder mask tenting over the via openings located on the back of the printed circuit board (PCB). In another configuration vias were removed from the center thermal pad and vacuum reflow performed during the liquidus phase of the solder with an explanation of why some of the voids remained. The first and second order results presented within this paper have practical implications and from their observations a novel process evaluation technique coined as Freeze Frame Reflow (FFR) was developed. In the last case study presented, an advanced mrQFN (multi-row QFN) package is investigated for factors affecting yields. FFR is then implemented resulting in an increase in yield further demonstrating the benefits this new & novel technique can offer.

Keywords: QFN, mrQFN, SMT, BLR, freeze frame reflow, Automotive Manufacturing, BTC, solder joint voids, fillet formation, oxidation, stencil technology, flux, X-ray reflow, video microscopy, cleaning chemistry, solder paste, IPC-A-610, IPC-7093, IPC-7351.

INTRODUCTION

The introduction of QFNs was one that initially created some market excitement due to its low profile and reduced form factor. In addition, the improved electrical and thermal properties offered by this package generated a high level of interest from the design community. This trend in low profile packages was further advanced with the introduction of the PicostarTM package by Texas Instruments as illustrated in Figure 1.

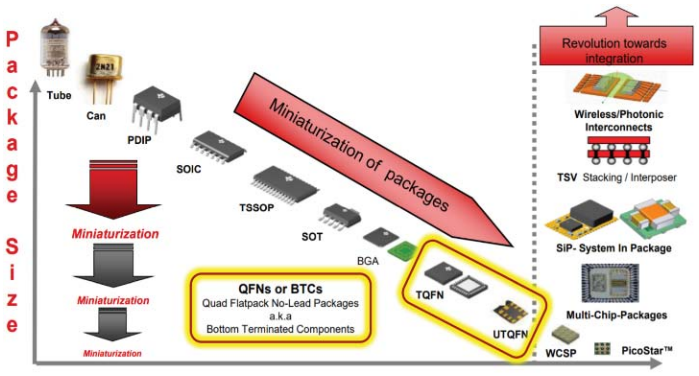

Figure 1: Density and Integration Improvements over Time.

The mobile and wearable electronic markets were the first to embrace embedded SIP (system in package) solutions for their optimized volumetric form factor incorporating an embedded PicostarTM package as illustrated in Figure 2.

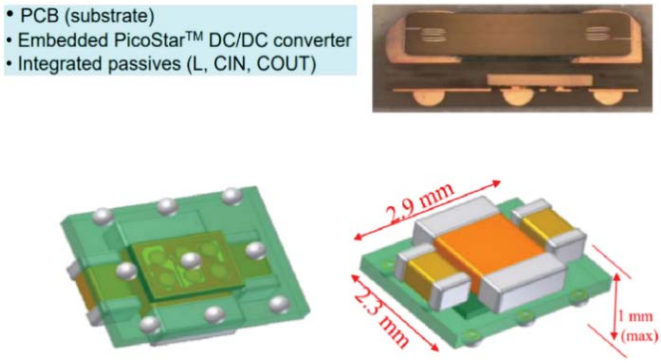

Figure 2: Package thickness progression enabling embedded solutions.

The reduction in thickness progression contributing to overall volumetric density shrink is illustrated in Figure 3.

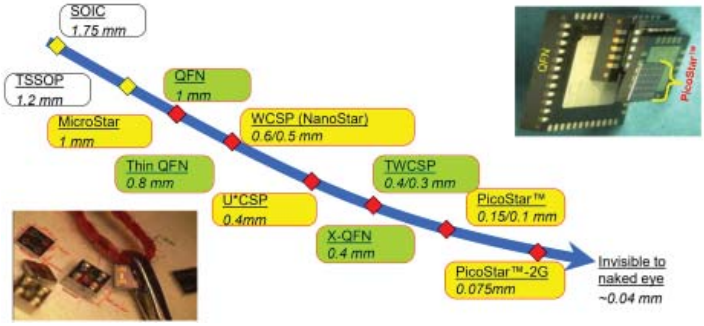

Figure 3: Package thickness progression enabling embedded solutions.

An appreciation for both the low-profile nature of BTC packages and the overall scales involved is illustrated in Figure 4 where a finished assembly cross section of a PicostarTM package mounted directly to a PCB are dimensioned. Note the silk screen marking is on the same order of magnitude as the package and solder standoff.

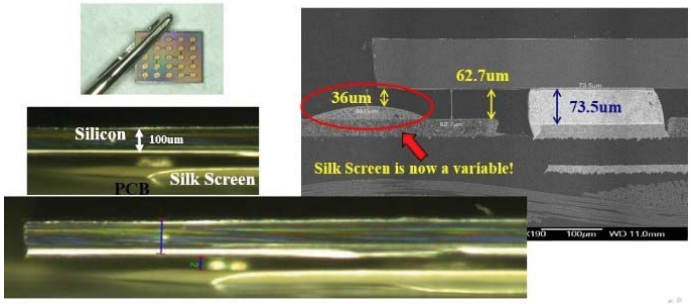

Figure 4: Picostar*TM* mounted on PCB

Like other low-profile components such as BGA's (Ball Grid Arrays), QFN packages have standoffs dictated by the volume of solder deposited however without the solder sphere volume offered by BGA interconnects therefore the quality of the solder joint geometry formed post assembly is paramount. The final standoff height, voiding within the solder joint, consistency of solder volume from screen printing, and tilting can impact the finished geometry of the BTC solder joint [1]. Industry quality standards have been developed to give guidance in addressing solder joint quality.

Regarding voiding of BTC's standards such as the IPC-A-610 and IPC-7093 offer guidance. IPC-A-610 simply states that the acceptance criteria need to be negotiated between the manufacturer and user [2]. While IPC-7093 recommends BTC periphery solder joints should have voids less than 25% which was originally established primarily for BGAs. In addition, the IPC-7093 does also mentions to limit the center thermal pad voiding to 50% or less. This 50% voiding criteria has a disclaimer that the thermal performance should not diminish significantly or the voiding criteria should be reduced further evaluated on a device by device basis.

The 50% max voiding is a reasonable criterion for thermal dissipation [4] however may not be suitable for consistent yields due to excessive tilting leading to yield issues. The periphery solder joint geometries should be inspected for compliance to the IPC-A-610 BTC solder joint quality criteria in addition to satisfying the voiding criteria.

A variety of factors can contribute to void formation in solderjoints such as flux outgassing, level of starting oxidation of the component or substrate, printed solder geometry, via in pad structures, and pcb finish. For packages such as BGA's, gullwing leaded devices, and even BTC's these factors can be categorized into four groups – Printing or Dispensing Factors, Reflow Factors, Substrate or Component Factors, and Solder Paste Factors [5]. Sweatman et al. offers a comprehensive fishbone diagram which illustrates these relationships and of particular interest is the volume printing factor for BTCs. This volume factor takes on another layer of complexity for BTCs such as a QFN or PowerPadTM gullwing leaded package which typically incorporates a thermal pad. Even though gullwing leaded packages are not typically considered to be a BTC the PowerPadTM located underneath the package body recategorizes it. The exposed pad on these two package types are larger by area compared to the terminals and therefore are more susceptible to voiding. A window pane stencil pattern as shown in fig. 6 is typical and may entrap a void in the interstitial gap regions during reflow simply by its design. This window pane printed geometry is a necessity for QFNs to reduce the overall printed solder volume in the thermal pad allowing the collapse and successful solder joint formation on the periphery leads. One other added advantage assuming the part is placed onto the solder paste without excessive force are the channels in the pattern allowing solvents to outgas prior to reflow. In the case of the gullwing leaded packages which incorporate a thermal pad, the standoff is fixed which creates a different type of voiding. Lack of metal load voiding occurs due to the printed volume of solder missing the required metal load to fill the interstitial gap completely. There needs to be a careful balance in the stencil aperture design for gullwing thermally enhanced packages since excessive volume underneath the part creates tilting and potentially solder defects [6].

EXPERIMENTAL SETUP

PCB Test Vehicle Configuration

Factors such as PCB thickness & copper density, solder alloy choice, type of organic laminate material, glass weave density, and mechanical hardware induced strain of the finished assembly can all affect the long-term solder joint reliability related to solder fatigue however any accelerated stress testing analysis performed without consistent solder joint quality will result in confounding data [7-12]. In order to better understand the variables that affect BTC package solder joint geometries a test vehicle was designed allowing for different variables to be tested. Finished solder joint geometries were modified by varying 1) through hole via design, 2) solder mask tenting techniques, 3) periphery and center thermal pad printed solder joint volumes, and 4) no-clean and water-soluble solder paste flux chemistry all using SAC 305 alloy type 4.5 powder size. Figures 5 & 6 illustrate the PCB test vehicle designed with an array of coupons.

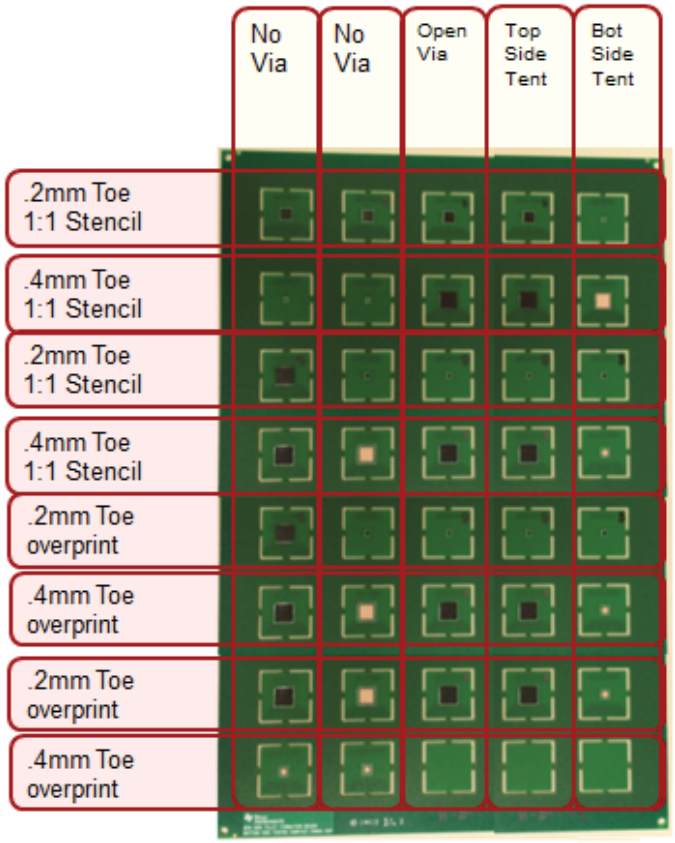

Figure 5: 1.6mm thick PCB Test Vehicle Layout.

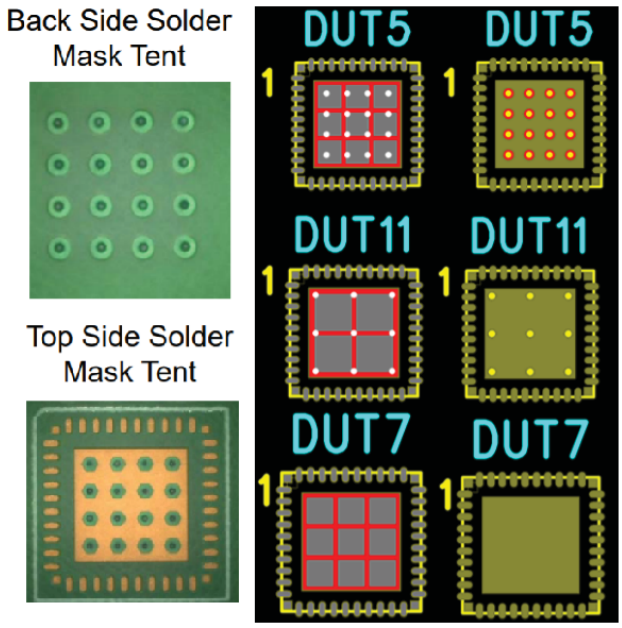

Figure 6: PCB test vehicle coupon layout examples with variations in the center stencil window pane pattern, vias, and solder mask tenting techniques.

Metrology Techniques & Observations

To better understand the influence of the variables listed above, a real-time observation approach was used. For visual observations a camera microscope was configured with a hot plate able to achieve reflow temperatures shown in Figure 7.

Figure 7: Keyence video microscope configured with hot plate.

An example of the reflow observation generated is illustrated in Figure 8. The standard land pattern was 1:1 underneath the QFN with a toe pad extending either 0.2mm or 0.4mm beyond the package perimeter. In combination with the land pattern both a standard aperture design was designed 1:1 with the land pattern and an extended stencil aperture (overprint of 0.2mm) extending beyond the toe of the periphery land pattern was designed. In addition, the device used in the evaluation was a 40pin VQFN with 0.5mm pitch with no-clean SAC305 & OSP finish used on the PCB.

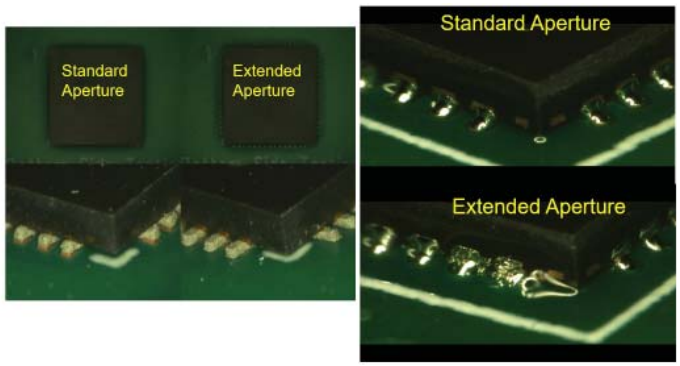

Figure 8: Standard Aperture and Extended Aperture pre and post reflow image. Outgassing corner bubble is present on lower right extended aperture image during reflow.

Several observations were made such as the molten solder volume located at the fillet would change geometry as the part oscillated up and down in the Z direction due to the outgassing of the flux underneath the component. The outgassing would manifest at the periphery as bubbles. An outgassing corner bubble can be seen in Figure 8 present on lower right extended aperture image during reflow. This bubble has a brightness aberration due to lighting effects during recording. Also, at the onset of reflow a substantial amount of liquified flux was present on the periphery which can be seen as a darker region present on each side about 2/3 towards the top of the QFN. Upon completion of reflow in the cooling phase the flux that was not vaporized during reflow would also draw back underneath the part. Note that all reflow observations were performed using ambient air without nitrogen purge therefore oxygen was present.

Another observation was fillet formation as a function of stencil thickness and periphery aperture design. Printed metal volume directly correlates to post reflow metal volume since by printed solder paste volume ~50% contains metal powder and the balance flux. Most apparent were the fillets using the 0.2mm overprinted stencil aperture opening. Figure 9 illustrates the overall fillet formation with varying volumes of solder.

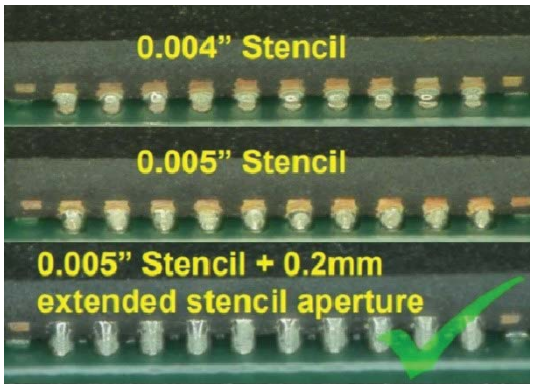

Figure 9: Side fillet formation as a function of solder volume including post high temperature bake and steam aging treatments.

Note that the extended aperture seems to give the most consistent fillet formation and also showed favorable wetting behavior on the un-plated side walls of the QFN package even after extended 150C bake and 8 steam aging as shown in Figure 10.

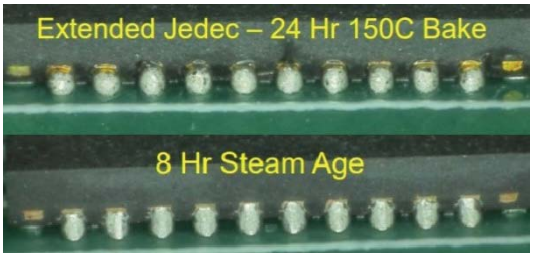

Figure 10: Side fillet formation as a function of solder volume including post high temperature bake and steam aging treatments.

Overprinting solder is not represented as an option in the IPC-7351 however does help to increase the opportunity for fillet formation. In this analysis the overprinting was limited to 0.2mm without any solder fines observed on the overprinted solder mask region indicating adequate paste activity to coalesce back into the bulk printed volume.

In combination with the live reflow video camera setup a real time X-ray reflow system was utilized to help correlate observations. In addition to live X-ray reflow capability, this system was also configured with vacuum reflow able to pull a vacuum down to 0.15 Bar. Figure 11 illustrates the live X-ray reflow system which uses an aluminum conduction plate to facilitate heating laterally to keep the heating elements outside the field of view of the X-ray during observations.

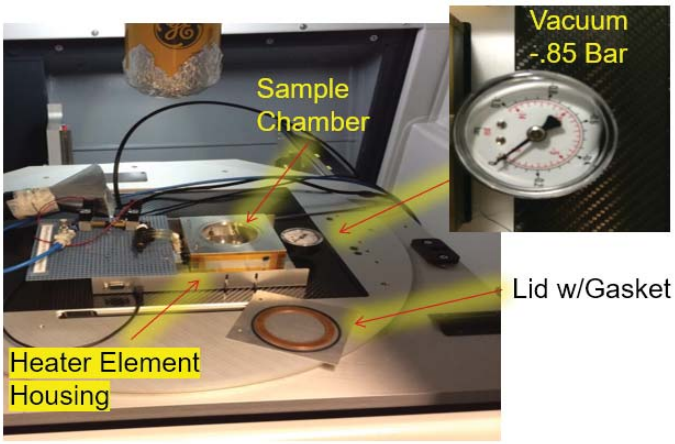

Figure 11: Live X-ray reflow system configured with Vacuum.

The vacuum reflow capability utilized a lid with gasket capable of pulling a vacuum down to 0.15 Bar or 15% of atmospheric pressure. In order to accommodate the limitation in the reflow chamber size the PCB was designed with an array of smaller coupon boards previously illustrated in Figure 5. These coupons were first printed, followed by component placement, then each coupon was carefully cut out and placed in the X-ray chamber for reflow.

The solder paste chemistry was also evaluated to insure consistent processing of the QFN parts thru SMT assembly. Two different solder pastes were evaluation subdivided into a SAC305 leadfree no clean and a SAC305 water soluble flux chemistry. Prior to populating the full factorial experiment the solder paste chemistries were observed thru live X-ray reflow to understand if there was a potential for noise that could be attributed to the material itself. A significant observation was the water-soluble chemistry produced much more outgassing to the point of generating defects during the preheat stage. The focus after this finding was to only use the no-clean chemistries to remove the noise attributed to pre-reflow paste movement. Figure 12 below illustrates the paste movement due to outgassing at ~200C which is below the liquidus temperature of the SAC305 alloy (217C~220C).

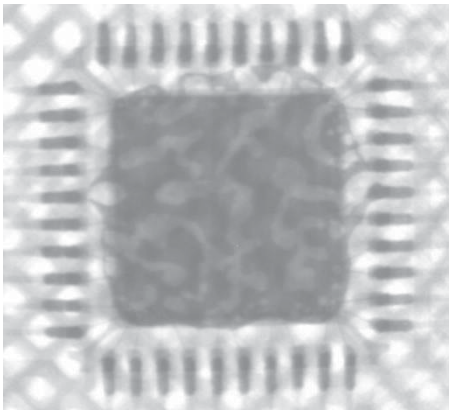

Figure 12: Water soluble paste X-ray observation at pre-liquidus temperature of 200C exhibiting significant migration of solder paste attributed to outgassing.

In comparison the low solids content no-clean flux chemistry didn't show much change in movement in the various coupons tested other than the back side tented via version as illustrated in Figure 13.

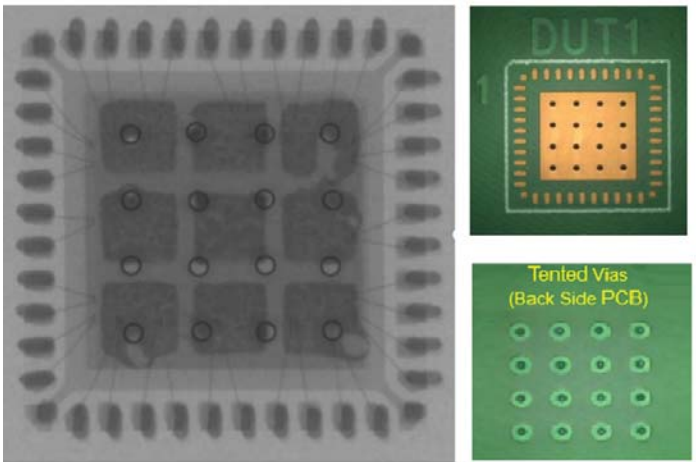

Figure 13: No-Clean 200C pre-reflow X-ray using backside tented vias on an OSP finished board.

The stencil used was 0.004" in thickness with 1:1 printed solder on the periphery using SAC 305 no-clean flux chemistry. In addition, a slight offset was introduced to illustrate the self-centering effect from the surface tension of the solder once reflow is achieved. The movement of solder paste in this case is more attributed to the air trapped in the backside solder mask tented vias vs. flux outgassing due to via proximity.

To explain this distortion the ideal gas law can be used and by substituting the variables to account for a constant number of moles (n) the combined gas law can be derived and is useful to determine the changes in volume as a function of temperate and pressure.

$$PV = nRT$$

$$\frac{P_1V_1}{T_1} = \frac{P_2V_2}{T_2}$$

This further simplifies to the form below under constant pressure.

$$V_2 = \frac{T_2}{T_1}V_1$$

By taking the ratio of temperatures and converting to Kelvin the expected ratio of volumetric change going from room temp ~23C to 200C will result in an expansion of ~1.6 times the starting volume. This expansion in volume within the tented vias capped by the solder paste will displace the printed solder volume during heating until it finds a path to outgas into the ambient environment.

In continuation of the same unit through reflow additional observations were recorded. For instance, the periphery fillet formation represented by the opaque X-ray signature would appear and disappear depending on the amount of voiding which correlated closely with the previous camera microscope observations where the part would oscillate in the Z direction as shown in Figure 14a where minimal voiding is seen. The upward Z axis movement of the part caused by the outgassing of solder paste flux through reflow caused the solder to thieve underneath as illustrated in Figure 14b. Once the array of voids connected and found a path to the periphery of the thermal pad the volume of gas released would allow the part to collapse back to a lower standoff resulting in the re-appearance of the periphery solder joint fillets. This also correlated closely with the camera microscope observations where outgassing in the form of flux bubbles were present in combination with the downward movement of the part. Lastly the voids present in close proximity to the vias would reduce in volume as the cooling phase of the reflow profile started. This progression in the reduction in void size during cooling would then freeze once the solidification temperature of the solder alloy is achieved as illustrated in figures 14c and 14d respectively.

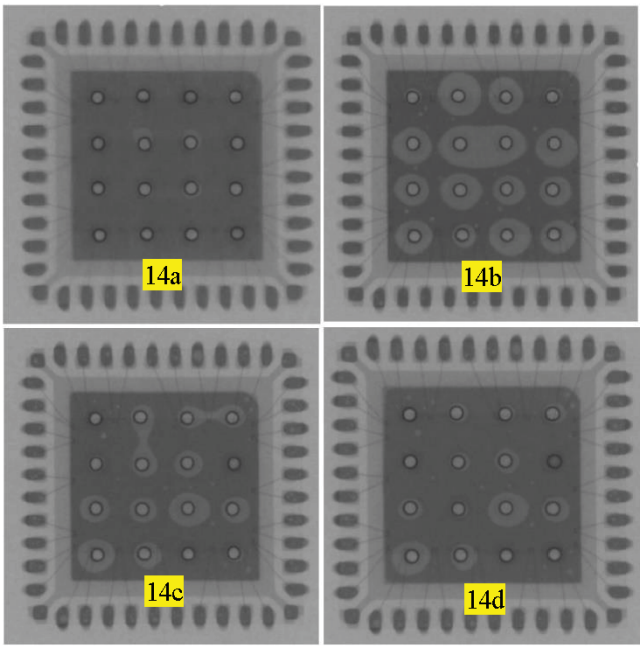

Figure 14: a. Onset of reflow just after melting, b. voiding increasing standoff height c. Peak reflow temp d. Peak to solidification temp.

In the next set of images, a test coupon without any vias using a 4-segment window pane thermal pad aperture pattern was evaluated through reflow with the addition of vacuum at different time intervals. The stencil thickness used was 0.005" in combination with a no-clean SAC305 solder paste. Illustrated in figure 15a is the initial X-ray view at room temperature where additional placement pressure was applied.

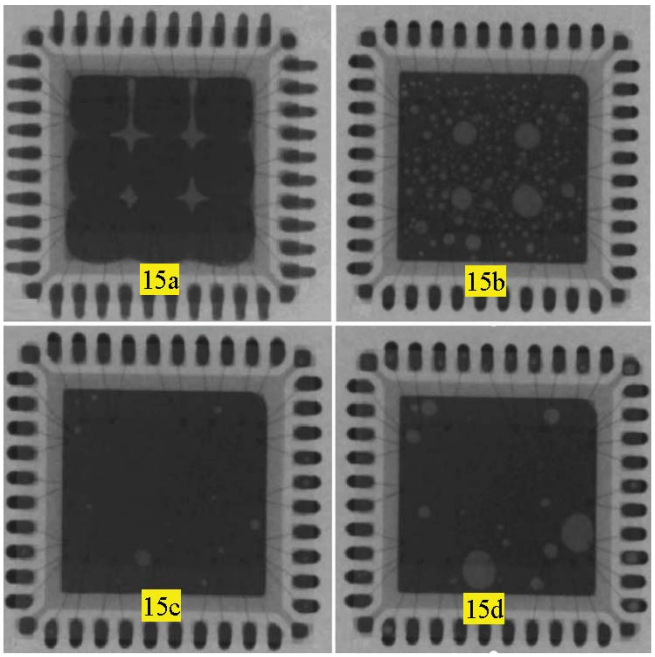

Figure 15: a. Initial pre-reflow X-ray b. Liquidus temperature reached c. Post vacuum at 0.15bar for 17 seconds d. re-applying vacuum.

Note how the squeeze out seems substantial in the center thermal pad region of the paste however the periphery leads have minimal distortion. Figure 15b captures an X-ray image immediately after the melting point of the SAC305 has been reached where the interstitial gaps from the original window pane pattern has contributed to the larger 4 voids due to the solder paste coalescing entrapping this initial volume of air. Figure 15c illustrates the results of applying 17 seconds of vacuum achieving 0.15 Bars of pressure. In observation once the vacuum was started the outgassing of voids progressed rapidly. Just as in the previous tented via case study before as the voids erupt from the perimeter of the thermal pad outgassing will occur. Figure 15d illustrates one last attempt to enlarge the voids by enabling the vacuum again but due to the inability of the void to reach the periphery of the liquidus solder it returns to its original size as shown previously in 15c.

Texas Instruments Freeze Frame Reflow Technique

From these observations a novel new approach to characterizing the solder paste interactions with low profile BTCs was realized. This new approach named Texas Instruments Freeze Frame Reflow (TIFFR or just FFR) offers any SMT assembly site that does not have a real time X-ray reflow system an option to characterize BTC solder paste chemistry interactions on site.

In order to perform FFR a sample PCB, the production stencil, and the BTC parts of interest should be allocated to this evaluation. The partial assembly comprising of just the BTCs mounted on the screen-printed boards should then be run through a modified reflow profile. The goal of this exercise is to achieve a reflow profile temperature just below the melting point of the solder alloy in order to observe any distortion or migration of the solder paste. Figure 16 illustrates an example reflow profile where the spike region has been clipped in order to avoid the plastic/liquidus phase of the solder alloy.

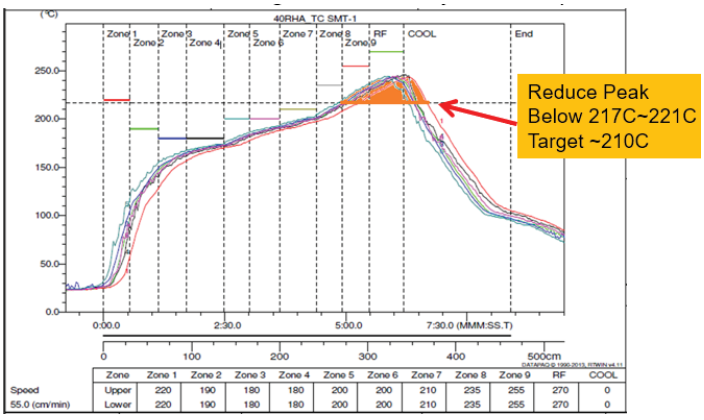

Figure 16: TIFFR example reflow profile.

Once the board exits the oven and cools to a safe temperature for handling a passive inspection should be done for any obvious defects followed by a standard 2D X-ray inspection. To better illustrate the TIFFR method a multi-row QFN (mrQFN) case study is investigated.

The context of the case study begins with ~70% fallout being seen at functional test where both shorts and opens are being identified. Even on passing units the mrQFN solder joints have an asymmetrical distribution of sizes where some are thieved and other have excessive volume. In this case study a type 4.5 powder water soluble SAC305 solder paste was used in combination with a 4mil stencil.

Figure 17a & b illustrates the first pass mrQFN samples using FFR. Figure 17a. was taken to ~200C peak and Figure 17b was taken much closer to liquidus at ~215C peak. Note the thermal couple locations were placed in a via near the package of interest. The voiding is significant in some regions in Figure 17a however the solder paste has not migrated beyond the printed region to the point of obvious defects. However, in Figure 17b it's apparent that not only shorts but opens will developed due to extensive migration of solder paste away from the initial well-defined print.

Since the flux can't be resolved using X-ray the method of prying is very helpful to examine flux residues on both the part and board. An optical image is shown in combination with figure 17b where the mrQFN device has been pried and flipped over to the left of the PCB land pattern to better relate the proximity of the defects.

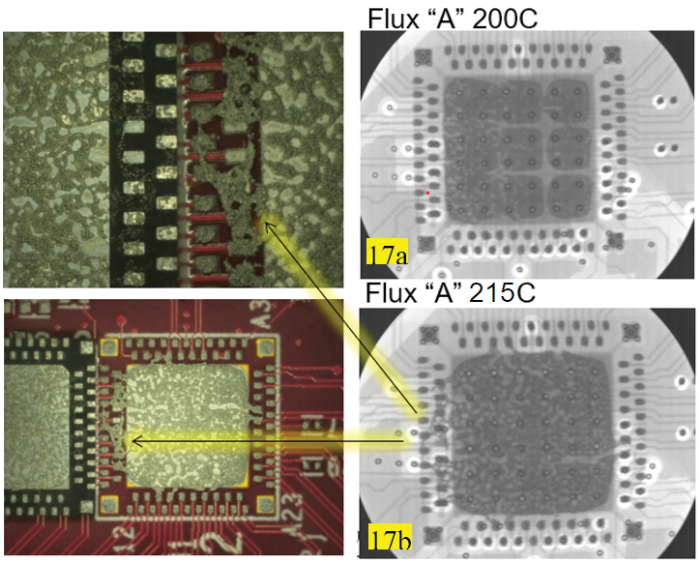

Figure 17: a. TIFFR mrQFN results at 200C b. TIFFR results at 215C.

From this finding several attempts were made to modify the profile with help from the solder paste manufacturer but no significant improvements could be made. The next step recommended was to change the flux chemistry to a low solid content SAC305 no-clean paste suitable for ambient air reflow. As illustrated in Figure 18 significant improvement can be seen in the ~215C FFR where the solder paste no longer migrates beyond the original printed region.

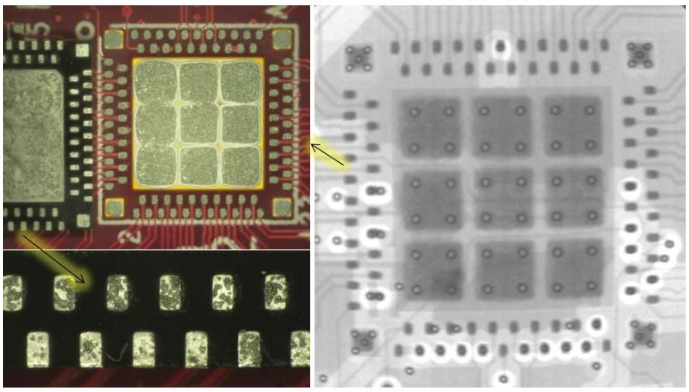

Figure 18: No-clean SAC305 solder paste results using FFR at ~215C.

On closer inspection both Flux A (water soluble) and Flux B (no-clean) were compared visually in Figure 19. The flux residues of A are significant compared to the flux residues from the no-clean paste B.

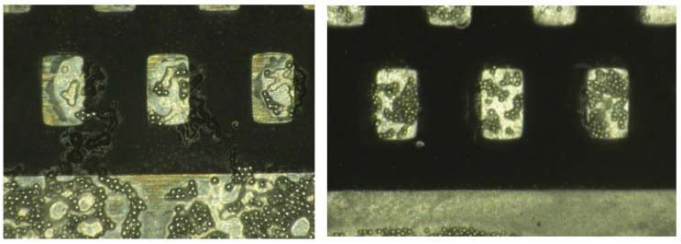

Figure 19: Side by side comparison of water soluble vs. no-clean FFR results respectively.

In order to verify robustness of this combination 10 additional mrQFN boards were run resulting in 0% fallout. Production was restarted with 100% passing results related to the mrQFN which also now exhibits consistent solder joints geometries when inspected in X-ray.

CONCLUSIONS

As the standoff heights and feature sizes of advanced BTC packages continue to progress to finer geometries the need for more advanced materials and metrology techniques to verify compatibility becomes apparent. Real time video and in-situ X-ray combined with reflow capability is an excellent tool to better understand the material interactions that occur with BTCs. For assembly sites without access to these types of tools the use of FFR becomes an invaluable technique to quickly identify BTC solder paste chemistry compatibility. FFR offers another tool in the SMT process engineers toolbox to help verify flux outgassing interactions through the use of a modified reflow profile which limits the peak temperature just below the liquidus temperature of the solder alloy being evaluated. Since flux is translucent to X-ray, prying the part from the board offers greater detail in observing flux residue interactions after performing FFR.

FFR becomes less advantageous to use with BTCs incorporating

a substantial standoff. For example, BGAs also have terminations located underneath the component however will have a solder sphere offering a standoff in excess of 6mils. This increased standoff coupled with a lesser amount of solder paste volume will not produce the same output signal of voiding as compared to the large volume of solder paste deposited on a QFN thermal pad. Due to these differences BGAs won't produce the same magnitude of voiding as seen with QFN's and the FFR technique would not be as advantageous in determining flux chemistry compatibility.

ACKNOWLEGEMENTS

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BIOGRAPHIES

Steven Kummerl received his B.S. degree in Mechanical Engineering from the University of Texas El Paso. He is a senior member of technical staff at Texas Instruments supporting semiconductor packaging with a focus in high power GaN & sensor technology. His career in electronics has spanned both the field of high volume/high mix surface mount assemblies for more than 13 years and over 19 years at TI supporting advanced packaging R&D. He holds over 45 patents in the field of package design and has authored numerous publications focused in packaging design, SMT package assembly, and reliability.

Bernhard Lange received his engineering degree in Electronic from the Applied Science University in Munich. He is an emeritus senior member of technical staff at Texas Instruments, supporting semiconductor new product qualifications and package development. He started his carrier 37 years ago with Texas Instruments as a Test Engineer, working the past 32 years in the Quality organisation and supporting SMT process questions from customer with new packages. He holds over 20 patents in the field of IC package design and assembly.

David Chin is a Packaging Engineer with Texas Instruments Worldwide Semiconductor Packaging Group in Santa Clara, California. His area of focus includes substrate-based modules development, package qualification, board level reliability and failure analysis, PCB land pattern and stencil for TI packages, customer adoption and surface mount support. He has a BSEE and MBA.

Ryan Huang is a senior engineer at Texas Instruments supporting semiconductor packaging with focus on solder die attach process. His career began as SMT process for 8 years and over 6 years at TI supporting advanced packaging R&D in electronics. He holds 2 patents in the field of package design. In his current role, he supports SMT process related issues, helps develop new manufacturing processes, troubleshoots production

issues, and does root cause analysis of failures related to soldering and die attached process.

Sreenivasan Koduri (KK), a TI Fellow, has helped define and drive our company's Analog packaging strategy for more than 20 years. He pioneered innovations such as copper wire-bonding, BOP-COA wafer-scale-package, HotRod™ packaging, embedded packaging and sensor packages – that have helped TI expand in the cost-competitive commodity market and in differentiated precision products. He also helped create and institute the Process, Package, Design IP and Test (PPIT) infrastructure that helps TI determine technology gaps and how to gain an edge over our competitors. KK currently is a technologist in SC Packaging.

KK's innovations are broadly fanned out and used in most of TI's Analog products. Many have also been adopted across the industry. These creative solutions have saved more than billion dollars for TI, and have significant impact for the entire semiconductor market.

Along with technology development, KK is passionate about developing talent. He has developed technical, managerial, and administrative leaders in multiple organizations across TI. He is a part of Tech-Ladder Leadership Council (TLLC) and is setting the strategy for TI's Tech-Ladder process. He is the chair of SMU Electrical Engineering school board, where he helps with development of staff and students.

KK has bachelor's, master's and doctorate degrees in Electrical Engineering, a master's degree in Business Administration and a master's degree in Finance.

Andy Zhang has been working with Texas Instruments since 2008 specifically in the area of board level reliability (BLR) testing and engineering, including BLR temperature cycle, drop/shock, bend, and vibration test, PCB design, and Surface Mount Technology. He is an active contributor for several IPC, AEC, and JEDEC standard task groups. He received his Ph.D. degree in materials engineering from Binghamton University.