Cu Conductive Pastes as Via Filling Materials for Various Substrates

Yoshinori Ejiri, Masumi Sakamoto, Chiaki Shimizu
Resonac Co., Ltd.
Ibaraki, Japan

ABSTRACT

Electrolytic Cu plating is commonly used as a filling technique for via holes in through silicon via (TSV), through glass via (TGV), and organic substrates. In order to miniaturize and increase the density of substrates, the vias are becoming smaller in diameter and have a higher aspect ratio. For vias with small diameters and high aspect ratios, voids in the electrolytic Cu plating film are issues. In this study, we developed a Cu paste that can be used as a filling material for TSV, TGV, and organic substrates without creating any voids and cracks. Non-through holes with diameters ranging between 20 and 100 µm and depths ranging between 70 and 100 µm (aspect ratios from 1 to 3.5) formed in a silicon surface layer were filled with Cu paste. TGV substrates with diameters ranging between 30 and 90 µm and thickness of 300 µm (aspect ratios from 3.3 to 10) were filled with Cu paste without voids and cracks. Multilayer substrates with the diameters of 180 and 260 µm and a thickness of 6.4 mm (aspect ratios: 25, 36) were filled with Cu paste without voids and cracks. The 2.5D chip package was prepared using a TSV filled with Cu paste as a 2.5D interposer. The 2.5D chip package was verified through reliability test [thermal cycle test (TCT), high temperature storage test (HTST), un-bias high accelerated stress test (HAST) and pressure cooker test (PCT)]. After the reliability tests, the conductive resistance of the package that adopted the Cu paste was found to be within 10% of the initial value. Moreover, we found that Cu paste can be applied to 2.5D interposer as filling material, too.

Key words: Low-temperature metallization, Cu paste, Via filling, TSV, TGV, Organic substrate

INTRODUCTION

Three-dimensional integrated circuits (3D ICs) and 2.5D ICs with silicon or glass interposers are considered to be promising candidates for overcoming the limitations of Moore's law owing to their advantages of low power consumption and high functional density1-2). An interposer is a rigid insulator layer that serves as an interface between the high I/O of various logic and memory dies and the lower-density substrate.

Through silicon vias (TSVs) and through glass vias (TGVs) are used in advanced 3D packaging solutions, such as the wafer-level packaging of microelectromechanical systems (Fig. 1 a), as well as silicon or glass interposers3-6 (Fig. 1 b). Cu is preferred as the filling material in TSVs and TGVs owing to its superior capability of filling large structures and its excellent electrical conductivity. Cu filling by electroplating is one of the cores and critical procedures in TSV and TGV fabrication. To reduce the number of voids in plated Cu, various studies have been conducted on plating conditions and additives7-9. However, the plating of the larger TSV and TGV structures often results in voids in the Cu filling 7-11, relatively thick outer surface layer plating8, and low productivity7, 10.

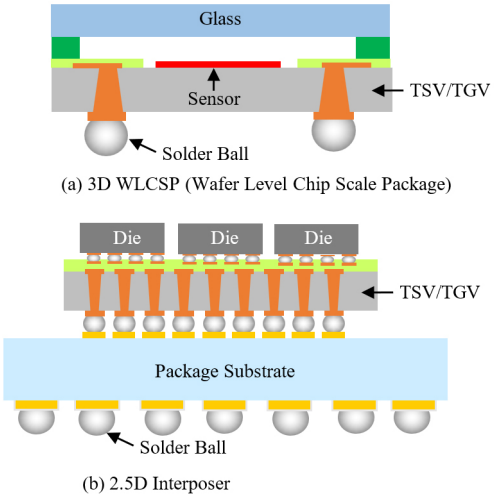
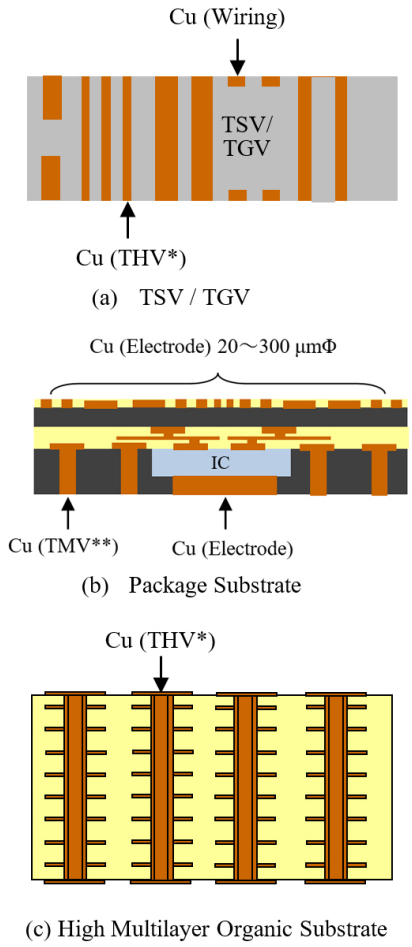


Figure 1: 3D Integration Technology

Therefore, we investigated the filling of vias of TSVs and TGVs with high aspect ratios using Cu paste, which results in few voids suppressing thick outer surface layer plating and provides high throughput. The Cu paste is made up of subµm- and µm-sized Cu particles, a small amount of µm-sized SnBi particles, and a solvent. Additionally, we examined the use of Cu for filling holes on organic substrates because this Cu paste can be sintered at temperatures lower than 230 °C. Potential application items of the Cu paste are shown in Fig. 2. We are targeting TSVs and TGVs in Fig. 2(a), as well as via hole filling and electrode formation in package substrates (Fig. 2b) and high multilayer organic substrates (Fig. 2c).



THV*: Through Hole Via, TMV**: Through Mold Via

Figure 2: Potential Applications of Cu Paste

EXPERIMENTAL PROCEDURES

Volume Resistivity Measurement

To investigate the effect of sintering conditions on the volume resistivity of the sintered Cu pastes, Cu films with a thickness of 60 μm and 1×5 cm in size were prepared and the volume resistivity was measured by four-terminal method using a Loresta-GX II MCP-T710 (Nittoseiko Analytech Co., Ltd). Cu film formation conditions are presented in Table 1.

Table 1: Cu Film Formation Conditions

Test Items	Details
Cu Paste	Subμm- and μm-sized Cu Particles, μm-sized SnBi Particles, Solvent
Sintering Temperature	150, 175, 200, 225, 250, 275, 300, 350 and 400 °C
Sintering Conditions	Formic Acid, 100%H_2

Via Filling Evaluation on Various Substrates

The experimental parameters for via filling experiments are presented in Table 2. Three types of substrates were prepared by via filling. When the via depth exceeds 1000 μm, formic acid does not penetrate into the center of the via and Cu paste becomes unsintered. On the other hand, 100% hydrogen penetrates more easily and has a higher reducing ability than formic acid for deep vias, organic substrate No. 3 in Table 2 with a via depth exceeding 1000 μm was sintered using 100% hydrogen.

Table 2: Process and Examination Items

No.	Substrate	Kind of Via	Via Diam. (μm)	Via Depth (μm)	Aspect Ratio	Via Filling Method	Sintering Condition
1	Si	Non-Thru Hole	20-100	70-100	1-3.5	Printing	Formic Acid 220°C (1 h)
2	Glass	Thru Hole	30, 60, 90	300	3.3-10	Press	Formic Acid 220°C (1 h)
3	Organic Substrate	Thru Hole	180, 260	6400	25, 36	Press	100%H_2 220°C (1 h)

(1) Si (TSV) – Blind Via

Blind vias with a diameters ranging between 20 and 100 μm and depths ranging between 70 and 100 μm (with aspect ratios from 1 to 3.5) formed in a silicon surface layer were filled with Cu paste. The overview of the Si wafer is shown in Fig. 3. A schematic of the vacuum printing method is shown in Fig. 4(a). The Cu paste was printed using a squeegee under vacuum and sintered at 220 °C for 1 h under a formic acid atmosphere.

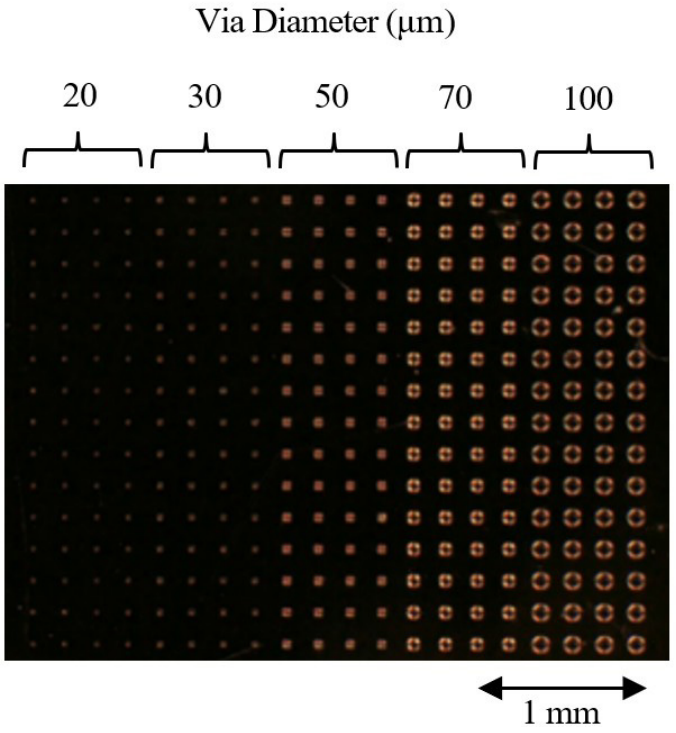


Figure 3: TOP View of Si Wafer

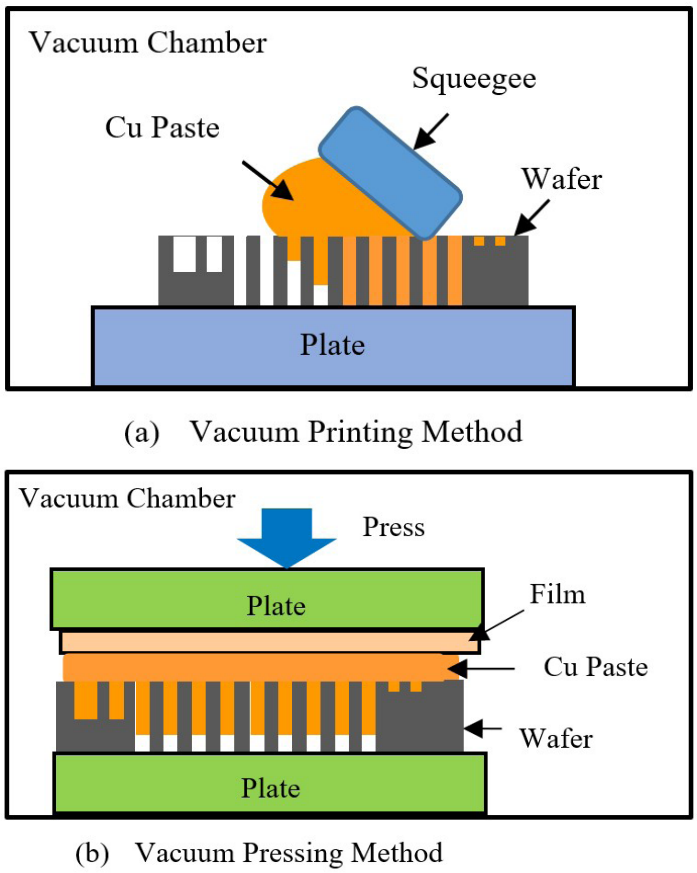


Figure 4: Process of Filling Holes by Cu Paste.

(2) Glass (TGV) – Through hole

TGV substrates with a diameter of 30, 60, 90 µm and a thickness of 300 µm were filled with Cu paste. The overview of the glass wafer is shown in Fig. 5. A schematic of the vacuum pressing method is shown in Fig. 4(b). Cu paste was applied to a PET film and pressed at a pressure of 0.3 MPa. The TSV substrates were sintered at 220 °C for 1 h under a formic acid atmosphere.

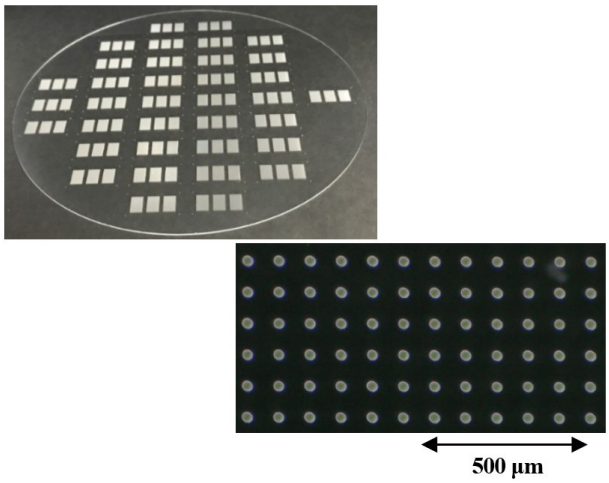


Figure 5: Top View of Glass Wafer.

(3) Organic substrate – Through hole

THVs with diameters of 180 and 260 µm and a thickness of 6.4 mm, in Multilayer substrates, were filled with Cu paste. These THVs had side walls shielded by an electroless Cu plating film were used. The -cross-sectional images of high multilayer organic substrate (before via filling) are shown in Fig. 6. Cu paste was applied to a PET film and pressed at a pressure of 0.3 MPa. Multilayer substrates were sintered at 220 °C for 1 h under a 100% hydrogen atmosphere.

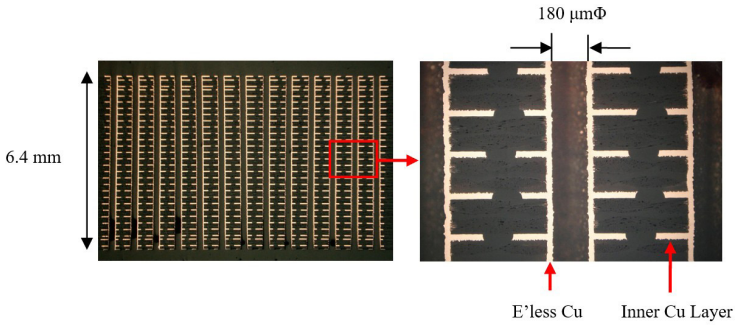


Figure 6: Cross-sectional Images of High Multilayer Organic Substrate. (Before Via Filling)

2.5D Integration with TSV Interposer

The-cross-sectional image of 2.5D integration with through Si interposer is shown in Fig. 7.

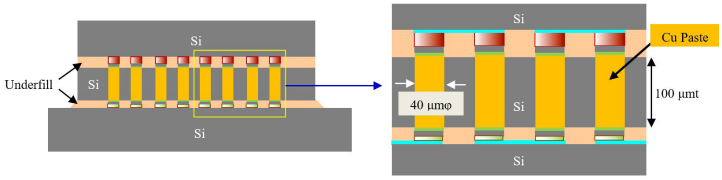


Figure 7: Cross-sectional Image of 2.5D Integration with Through Si Interposer.

TSV substrates with a diameter and thickness of 40 µm and 100 µm, respectively, were filled with Cu paste. The Cu paste was printed using a squeegee under vacuum and sintered at 220 °C for 1 h under a formic acid atmosphere. The Cu surface filled in the via of the TSV substrates was coated with electroless Ni (5 µm)/Au (0.05 µm) (ENIG: electroless Ni/immersion Au) plating. Si wafers with Cu pillars capped with Sn-3.5Ag and TSV substrates were connected by passing them through a nitrogen-reflow furnace. Subsequently, a Si wafer with electrodes formed with electroless ENIG plating and the TSV substrates were connected by a Sn-3.0Ag-0.5Cu (SAC305) solder paste passing through a nitrogen-reflow furnace. Finally, the underfill material was applied to both the sides of the TSV substrates. The 2.5D chip package was subjected to reliability test (TCT, HTST, HAST and PCT). The detailed test conditions are presented in Table 3.

Table 3: Reliability Test Conditions.

Test Items	Details
TCT	-55°C, 125°C/ 1000 cycles
HTST	150°C / 1000 h
HAST	130°C, 85%RH / 96 h
PCT	121°C, 100%RH / 96 h

RESULTS AND DISCUSSION

Volume Resistivity of Cu Films

The volume resistivity of Cu films as a function of sintering temperature and atmosphere is shown in Fig. 8. Comparing the atmosphere of formic acid and 100% hydrogen, 100% hydrogen is effective in obtaining lower volume resistivity Cu films. This result showed the film with the lowest volume resistivity of approximately 6.4 μΩ•cm was obtained at 350 °C or higher in 100% hydrogen atmosphere.

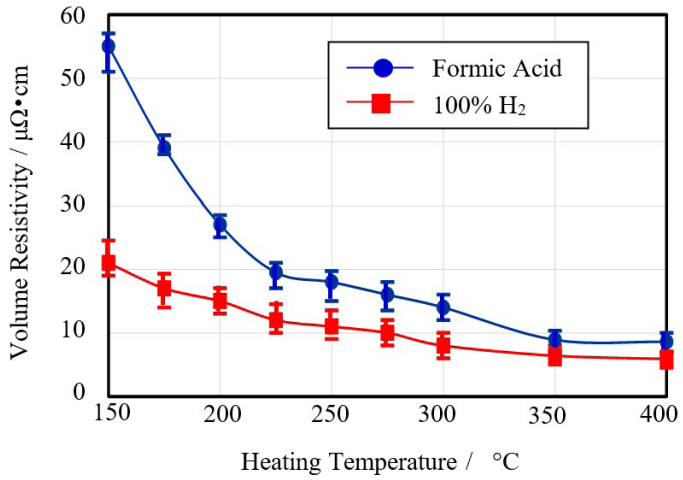


Figure 8: Volume Resistivity of Cu Films as a Function of Sintering Temperature. Sintering Atmosphere: Formic Acid, 100% H_2

Cu Filling State Based on Substrate Type

(1) Si (TSV) – Non-through hole

Cross-sectional images of the TSV filled with Cu paste are shown in Fig. 9. The enlarged view of each via in Fig. 9 is shown in Fig. 10. The holes can be filled with Cu paste regardless of via diameter and depth. In fact, the vias with a small diameter and high aspect ratio (via diameter: 20 μm, aspect ratio: 3.5) can be filled with Cu paste without inducing cracks or voids. The gray spots are solder and the black spots are small voids. By dispersing solder in the Cu film and forming small voids in a dispersed manner, it was possible to suppress the occurrence of cracks and large voids in the Cu film. Via opening was flat regardless of the via volume ratio. We infer that the CMP (Chemical Mechanical Polishing) process can be omitted using the Cu paste.

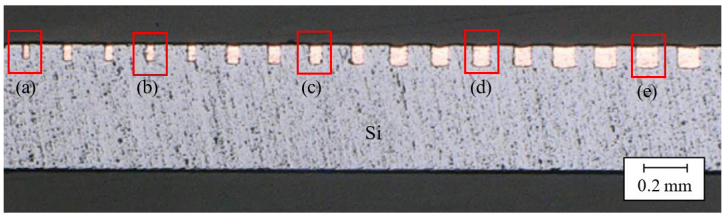


Figure 9: Cross-sectional Images of TSV Filled with Cu Paste. Via Diameter: (a) 20 μm, (b) 30 μm, (c) 50 μm, (d) 70 μm, (e) 100 μm Filling Method: Vacuum Printing, Metallization Atmosphere: Formic Acid, Temp.: 220 °C, Heating Time: 1 h

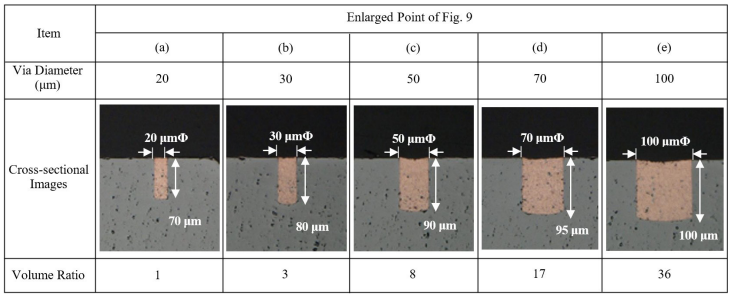


Figure 10: Cross-sectional Images of TSV Filled with Cu Paste. Filling Method: Vacuum Printing, Metallization Atmosphere: Formic Acid, Temp.: 220 °C, Heating Time: 1 h

(2) Glass (TGV) - Through hole

TGVs with a diameter of 30, 60, 90 μm and a thickness of 300 μm were filled with Cu paste. TSVs with a small diameter and high aspect ratio can be filled without inducing cracks, as shown in Fig. 11. In regard to the TGV (Fig. 11), the via diameter at the center of the substrate was narrower than the opening diameter, and the vias were filled with Cu paste without inducing cracks.

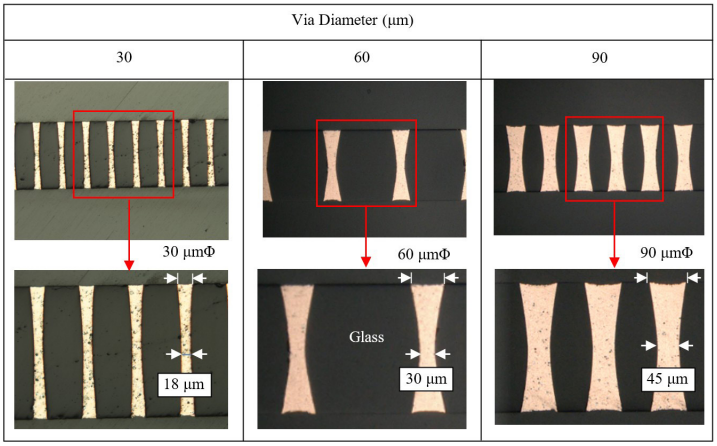


Figure 11: Cross-sectional Images of TGV Filled with Cu Paste. Filling Method: Vacuum Pressing, Metallization Atmosphere: Formic Acid, Temp.: 220 °C, Heating Time: 1 h, Thickness: 300 μm

(3) Organic substrate - Through hole

Multilayer substrates with a diameter of 180, 260 μm and a thickness of 6.4 mm were filled with Cu paste (Fig. 12). Fig. 13

shows an enlarged view of the central part and opening of the cross section of multilayer substrates with a diameter of 260 µm. As shown in Fig. 13, Cu paste can be formed without cracking, even when using a thick organic substrate and high-aspect ratio vias. Therefore, we conclude that Cu paste can be applied to substrates that require a high current density and high heat dissipation.

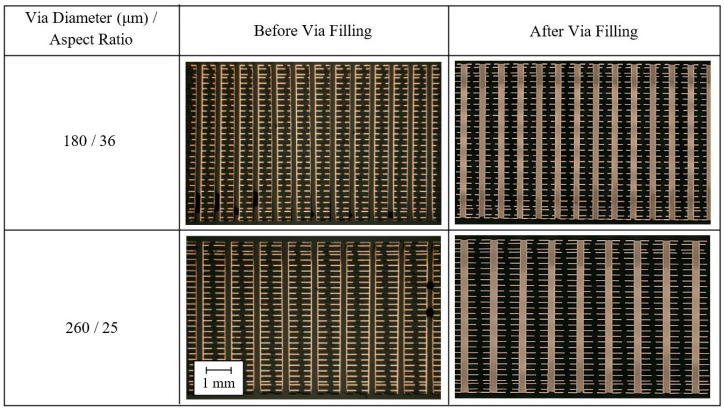


Figure 12: Cross-sectional Images of High Multilayer Organic Substrates Filled with Cu Paste.
Filling Method: Vacuum Pressing, Metallization Atmosphere: H2, Temp.: 220 °C, Heating Time: 1 h, Thickness: 6.4 mm

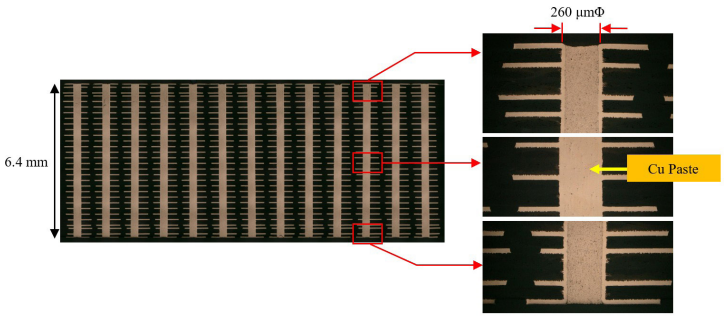


Figure 13: Cross-sectional Images of High Multilayer Organic Substrates Filled with Cu Paste.
Filling Method: Vacuum Pressing, Metallization Atmosphere: H2, Temp.: 220 °C, Heating Time: 1 h
Thickness: 6.4 mm, Via Diameter: 260 µm

2.5D Integration with TSV Interposer

TSVs, with a diameter and thickness of 40 µm and 100 µm, respectively, in Interposer substrates, were filled with Cu paste. The overview and cross-sectional images of the TSV substrate are shown in Fig. 14(a). The vias were filled with Cu paste, and no cracks were observed. The overview and cross-sectional images of the TSV substrate applied with ENIG on the Cu surface are shown in Fig. 14(b). The electroless Ni plating film was deposited directly on the Cu paste, and no extraneous deposition was performed on the Si wafer. The 2.5D chip package was prepared using a TSV-plated substrate as a 2.5D interposer. The overview and cross-sectional images of the electrodes connected via soldering are shown in Fig. 14(c). It was found that, there was robust wetting between the Cu-filled vias and ENIG plating during soldering (Sn-3.5Ag and SAC305), and no peeling occurred between the Cu paste and the electroless Ni plating film. The underfill material is applied to both the sides of the TSV substrates. The 2.5D chip package was subjected to reliability tests and the conductive resistance changing rate was within 3% in all tests (Table 4). The TCT results were specifically shown in Fig. 15. After 1000 cycles of TCT test, the conductive resistance increased about 1% over the initial resistance value and was within 3% of the target. The cross-sectional images of Cu paste and solder joint point after 1,000 cycles of TCT test is shown in Fig. 16. After the TCT test, there was no change in the Cu paste layer and the joint between Cu paste and electroless Ni-P compared to before the TCT test. We found out that Cu paste can be applied to 2.5D interposer as filling material.

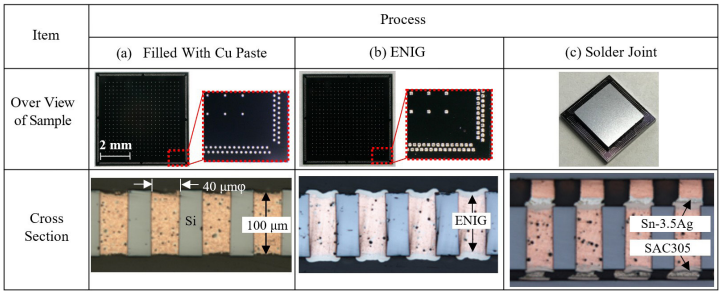


Figure 14: 2.5D Integration with Through Si Interposer.

Table 4: Reliability Test Results.

Test Items	Details	Resistance Changing Rate (vs. Initial Calue)
TCT	-55°C, 125°C/ 1000 cycles	within ±3%
HTST	150°C / 1000 h	within ±3%
HAST	130°C, 85%RH / 96 h	within ±3%
PCT	121°C, 100%RH / 96 h	within ±3%

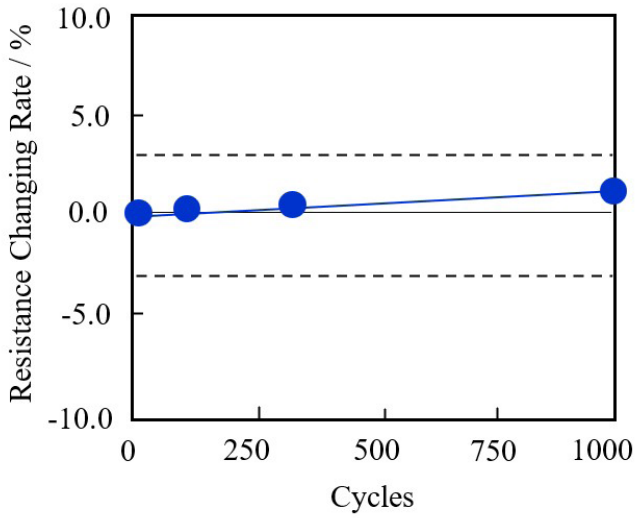


Figure 15: TCT Results of 2.5D Chip Package.
[Failure Criteria (Dashed Line): within ±3%]

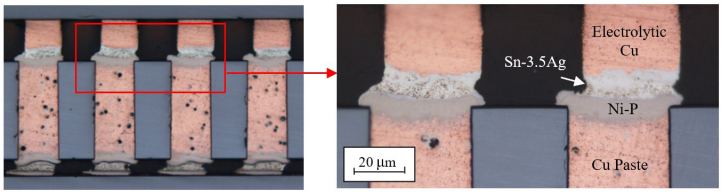


Figure 16: Cross-sectional Images of Cu Paste and Solder Joint Point after TCT Test (1000 cycles).

CONCLUSION

We developed a Cu paste that can be used as a filling material for TSVs, TGVs, and organic substrates. The following key conclusions are obtained:

(1) The film with the lowest volume resistivity of approximately 6.4 μΩ•cm was obtained at sintering temperatures of 350 °C or higher in an hydrogen atmosphere.

(2) Non-through holes with diameters of 20–100 μm and depths of 70–100 μm (aspect ratios from 1 to 3.5) formed in a silicon surface layer were successfully filled with Cu paste with no cracking or voids observed after sintering.

(3) TGV substrates with a diameter of 30, 60, 90 μm and a thickness of 300 μm (aspect ratios from 3.3 to 10) were filled with Cu paste without inducing cracks.

(4) It was found that Cu paste can be used to fill vias in various substrates without inducing cracks after sintering, even when using a thick and high-aspect-ratio organic substrate (thickness: 6.4 mm; aspect ratio: 25, 36).

(5) The 2.5D chip package was prepared using a TSV filled with Cu paste as a 2.5D interposer. After the reliability test, the conductive resistance of the package was found to be within 10% of the initial value. We concludes Cu paste can be successfully applied to 2.5D interposer as filling material.

REFERENCES

[1] S. W. Ho, S. W. Yoon, Q. Zhou, K. Pasad, V. Kripesh, J. H. Lau, "High RF performance TSV silicon carrier for high frequency application", In Proceedings of the Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, USA, 27–30 May 2008, pp. 1946~1952

[2] S. Koester, A. Young, R. Yu, S. Purushothaman, K. Chen, D. La, N. Rana, L. Shi, M. Wordeman and E. Sprogis, "Wafer-level 3D integration technology", IBM J. Res. Dev., 52, 2008, pp. 583~597

[3] J. H. Lau, "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging", ASME Journal of Electronic Packaging, 141(12), 2019, p. 040801

[4] R. Delmdahl and R. Paetzel, "Laser Drilling of High-Density Through Glass Vias (TGVs) for 2.5D and 3D Packaging", J. Microelectron. Packag. Soc., 21(2), 2014, pp. 53~57

[5] M. J. Laakso, J. Liljeholm, A. C. Fischer, G. Stemme, T. Ebefors, and F. Niklaus, "Maskless manufacturing of through glass vias (TGVs) and their test structures", In Proceedings of IEEE 30th Int. Conf. Micro Electro Mech. Syst. (MEMS), Las Vegas, NV, USA, Jan. 2017, pp. 753~756

[6] P. Dixit and K. Henttinen, "Via technologies for MEMS", In Handbook of Silicon Based MEMS Materials and Technologies, M. Paulasto-Kröckel, Ed., 2nd ed. Amsterdam, The Netherlands: Elsevier, 2015, ch. 38, pp. 694~712

[7] D. Josell, L. A. Menk, A. E. Hollowell, M. Blain and T. P. Moffat, "Bottom-up Copper Filling of Millimeter Size Through Silicon Vias", Journal of Electrochemical Society, 166(1), 2019, pp. D3254~D3258

[8] Q. S. Zhu, X. Zhang, C. Z. Liu and H. Y. Liu: "Effect of Reverse Pulse on Additives Adsorption and Copper Filling for Through Silicon Via", Journal of The Electrochemical Society, 166(1), 2019, pp. D3006~D3012

[9] R. P. Schmitt, L. A. Menk, E. Baca, J. E. Bower, J. A. Rpmero, M. B. Joordan, N. Jackson and A. E. Hollowell: "Void-free Copper Electrodeposition in High Aspect Ratio, Full Wafer Thickness Through-Silicon Vias with Endpoint Detection", Journal of The Electrochemical Society, 167, 2021, p. 162517

[10] P. Ogutu, E. Fey and N. Dimitrov: "Superconformal Filling of Through Vias in Glass Interposers", ECS Electrochemistry Letters, 3(8), 2014, D30-D32

[11] F. Zhao: "Improvement of Fully Filled Through Silicon Vias by Optimized Sputtering and Electroplating Conditions", Materials, 12, 2019, p. 3713