

## Journal of Surface Mount Technology

### Volume 37, Issue 3, 2024

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### Journal of Surface Mount Technology

June 2024 | Volume 37, Issue 3

ISSN: 1093-7358

6600 City W Parkway, Suite 300 Eden Prairie, MN 55344, USA

Phone: +1 952-920-7682 journal@smta.org www.smta.org

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In this issue, we bring you three interesting technical articles. The first paper explores the intermediate barrier performance of electroless Co-W-B and Ni-P stacked deposits. We follow that with a look at a cleaning process simulation using glass test boards. The final paper compares electromigration in tin-bismuth planar and bottom terminated component solder joints.

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The Journal of SMT is a quarterly, peer-reviewed, technical publication of articles related to electronic assembly technologies, including microsystems, emerging technologies, and related business operations.

# The Intermediate Barrier Performance of Electroless Co-W-B / Ni-P Stacked Deposits Between Cu and Solder Joint

### Yoshihito Ii, Hiroki Okubo, Shoichi Fukui, Tetsuji Ishida, Shoji Iguchi, Katsuhisa Tanabe and Shigeo Hashimoto

C. Uyemura & Co., Ltd. Osaka, Japan

#### **ABSTRACT**

Nickel (Ni) is one of the most common surface finishing materials for solder joint and wire bonding because it can behave as the diffusion barrier for Copper (Cu) and bring excellent reliability. Electroless Ni plating has many advantages such as high productivity, good thickness uniformity, and the deposition ability for isolated patterns of printed circuit boards without supplying electrolytic power. Electroless Ni plating is widely used as the jointing material for Tin (Sn) or Sn alloy solder in printed circuit boards, lead frames, and so on. The amorphous deposits of electroless Nickel-Phosphorus (Ni-P) generate the intermetallic compounds (IMC) with solder after the reflow and the remaining Ni behaves as the barrier between Cu and solder. In this time, the P amount of Ni-P deposits generally have the impact to the growth of IMC. Electroless Ni-P with high P (high P Ni) such as 10-12 wt% has been selected to achieve both corrosion resistance and solder joint reliability. Because the growth of Sn-Ni IMC between high P Ni is faster than deposits with lower P, the target thickness of high P Ni has been set to approximately 10 µm to sustain the Ni-P layer as the barrier layer between Cu and solder during reflow. However, if the Ni-Sn IMC is repeatedly formed and dissolved by the diffusion after solder jointing, the Ni-P layer reduces and finally disappears . As a result, an additional barrier layer is desirable for higher reliability. In this study, we investigated adding electroless Cobalt-Tungsten-Boron (Co-W-B) as a new intermediate barrier between Cu and solder jointing. We evaluated the bonding strength and IMC analysis after mounting Sn-Cu-Ni-P type solder on Cu/Co-W-B/Ni-P by using different reflow profiles. Results showed that Co-W-B 0.1-0.2 µm/Ni-P 1-2 µm stacked deposits had excellent bonding strength even though the Ni-P thickness is thinner such as 1 µm. After mounting solder, a P-rich layer was generated on the Co-W-B layer in cross-sectional Transmission Electron Microscope (TEM) observation. Scanning Transmission Electron Microscope (STEM) -Energy Dispersive X-ray Spectroscopy (EDS, STEM-EDS) analysis showed the P-rich layer and Co-W-B layer prevented diffusion between solder and Cu. Furthermore, even if after the thermal loading of high temperature, the bonding strength was excellent. Additionally, the cross-section analysis of STEM-EDS

revealed that a thin layer composed of Ni, Co and P was formed between Co-W-B and the P-rich layer. This thin layer also might behave as the barrier for solder. In conclusion, Co-W-B / Ni-P stacked deposits exhibited excellent reliability as the additional intermediate barrier layer between Cu and solder.

Key words: Electroless Co-W-B, Electroless Ni-P, barrier metal, solder joint

### **INTRODUCTION**

Ni is used as the surface finishing material for solder jointing widely because it can make intermetallic compounds with solder and provides excellent bonding strength[1,2]. Especially, electroless Ni has benefits as the aspect of productivity or deposition ability for isolated pads without electrolytic power supply. Electroless Ni deposits generally include co-deposited P and this P content has effects for solder jointing.

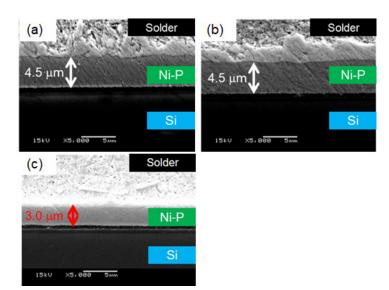


Figure 1: Typical cross-sectional SEM image after soldering with Ni-P 5  $\mu$ m deposits which have each P amount (5k). (a) P 2-4 wt.%(Low P), (b) P 6-8 wt.% (middle P) and (c) P 10-12 wt.%(High P). The solder is a Tin-Silver-Copper (Sn-Ag- Cu) type and soldering under 280 °C, 8 min reflow.

Figure 1 shows high P Ni has faster consumption thickness by the solder joint compared with Low P or Middle P type deposits due to much affinity to the solder[3]. However, high P Ni has excellent corrosion resistance properties. Therefore, the target thickness is set thicker such as 10 µm for the solder jointing application using corrosion resistant high P Ni so that a barrier between Cu and solder can remain.

On the other hand, electroless Co-W-B deposits were evaluated for the thermal diffusion barrier of the semiconductor Cu wiring in some papers[4-6]. According to these studies, it demonstrated the barrier ability under 400 °C[5].

Based on this background, we investigated to add a Co-W-B layer between Cu and high P Ni as the intermediate barrier between Cu and solder.

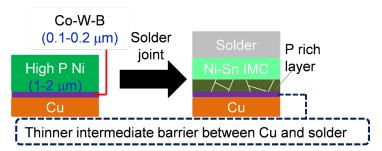


Figure 2: Co-W-B / high P Ni stacked deposit and after solder joint structure.

Figure 2 shows our proposal in this investigation. The Co-W-B is anticipated to act as the stronger and thinner barrier instead of high P Ni. The high P Ni thickness could be thinner because it is only needed for generating the IMC with solder.

In this study, we evaluated the bonding strength, the barrier ability, and detailed cross sectional structural analysis after solder jointing with Co-W-B / high P Ni stacked deposits.

### **EXPERIMENTAL**

In this investigation, C1100P Cu test pieces were used as the substrates. The Cu test pieces were plated using the process below.

Table 1: Electroless Co-W-B / high P Ni plating process

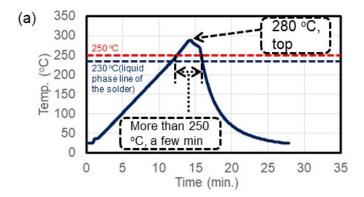
Process	chemical	temp (°C)	Time (min)
Cleaner	Mild acid type	50	3
Micro etching	100 g/L SPS	25	1
Acid rinse	10% H <sub>2</sub> SO <sub>4</sub>	r.t.	1
E-less Co-W-B	W:35-65wt.%/B: 0-0.2 wt.%	73	16(for 0.1 μm)
E-less Ni	High P type(P 10-12wt.%)	90	4(for 1.0 μm)

In this process, the Palladium (Pd) activation wasn't needed for the Cu substrate because dimethylamine borane (DMAB) which was in the electroless Co-W-B chemical as the reducer had catalytic ability on Cu surfaces and it allowed deposits on Cu directly. The Co-W-B deposit or Co-W-B / high P Ni deposition status was evaluated by Focused Ion Beam Scanning Electron Microscope (FIB-SEM, XVision 210 DB, Hitachi high-tech). Moreover, elemental

analysis of the Co-W-B deposit was performed by Auger Electron spectroscopy (AES, JAMP-9500F, JEOL).

The plated test pieces were solder jointed with Sn-Cu-Ni-P type solder by below Figure 3 (a) or (b) condition respectively under N2-formic acid atmosphere.

One of the purposes for this Co-W-B / Ni-P stacked deposits is to apply for the automotive electronics which high melting point solder is generally used for solder jointing. Therefore, these high temperature reflows which were shown in Figure 3 (a) or (b) were chosen for this investigation even though it can work under the low temperature reflow.



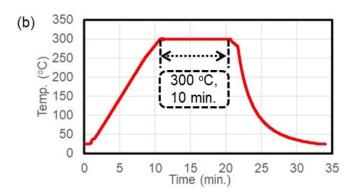


Figure 3: Reflow profiles for soldering with Co-W-B / high P Ni (a) 280  $^{\circ}$ C, top (b) 300  $^{\circ}$ C, 10 min.

After solder joining with a nut which was coated with electro Ni on iron (φ 5 mm) by the above reflow conditions, these were evaluated for bonding strength and fracture mode by the load tester (MODEL-1311VC, AIKOH ENGINEERING). Moreover, the plating test pieces with mounted solder were evaluated for the cross-sectional status by Scanning Electron Microscope (SEM, JSM-7800F, JEOL). The detailed structural analysis and elemental analysis was performed by Transmission Electron Microscope (TEM, JEM-F200, JEOL) and attached Energy Dispersive X-ray Spectroscopy detector (EDS, JED-2300T, JEOL).

Cross-section polishing for SEM was performed by ion milling system (IM-4000, Hitachi high-tech). The TEM specimen preparation was performed by FIB-SEM (XVision 210 DB, Hitachi high-tech).

### **RESULTS AND DISCUSSION**

Preparation of electroless Co-W-B or Co-W-B / high P Ni deposit

The electroless Co-W-B deposit was deposited directly on Cu. Figure 4 shows the cross-sectional backscattered electron (BSE) image of Co-W-B deposit and its AES depth profile analysis.

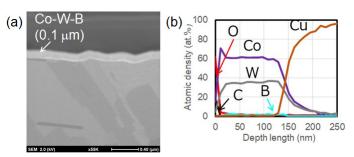


Figure 4: The deposition status and elemental analysis of Co-W-B deposit. (a) The cross-sectional BSE image (55k) (b) AES depth profile analysis.

Figure 4 (a) shows uniform deposition of Co-W-B without any defects such as voids. Figure 4 (b) shows the W and B content in Co-W-B deposit. Based on Figure 4 (b), the Co, W, B contents value, which was 54 nm for the depth length were Co:63.4 at.%, W:34.86 at.%, and B:1.74 at.% respectively. Therefore, these values were Co: 36.76 wt.%, W: 63.05 wt.% and B: 0.20 wt.%.

Moreover, Figure 5 is the cross-sectional BSE image of Co-W-B / high P Ni stacked deposits. It also shows that high P Ni could deposit on Co-W-B properly.

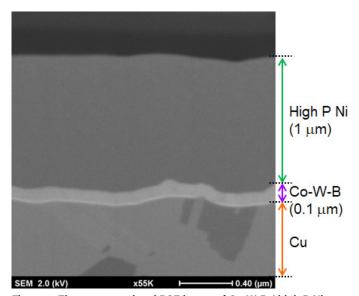


Figure 5: The cross-sectional BSE image of Co-W-B / high P Ni stacked deposits (55k).

### The evaluation of the bonding strength

First of all, the bonding strength and its fracture mode in the various deposits after soldering with Figure 3 reflow profile was evaluated by the nut pull test. The procedure is illustrated in Figure 6.

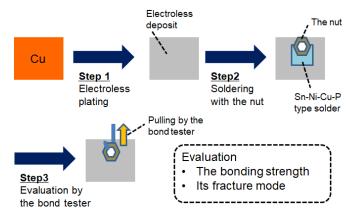


Figure 6: The nut pull test procedure

The list of electoless deposits, applied reflow profile for solder joint and evaluation results are shown in Table 2.

Table 2: The list of electroless deposits, reflow profile which used for solder jointing and the evaluation result of bonding strength by the average of three tests.

lan	Co-W-B	B High P Ni Reflow profile Bonding strength (N)			fracture			
leg	(μ <b>m</b> )	(μ <b>m</b> )	for solder joint	N1	N2	N3	Ave.	iracture
1	0	10		875	1003	930	936	solder
2	0	1	280 °C top		487	382	435	solder/Cu
3	0.2	1		1117	936	939	997	solder
4	0.2	1	300 °C, 10 min	908	791	1032	910	solder

The thicker high P Ni single deposit showed excellent bonding strength, however thinner such as 1  $\mu$ m thickness of high P Ni single deposit was unable to keep the bonding strength and fractured between solder and Cu.

However, when 0.2  $\mu$ m of Co-W-B deposit was added between Cu and 1  $\mu$ m of high P Ni deposit, the bonding strength showed improvement. Moreover, these stacked deposits kept excellent bonding strength and good fracture mode despite applying harder reflow profile which is shown Figure 3 (b). In conclusion, adding the Co-W-B layer was effective in keeping excellent bonding strength under thinner high P Ni conditions.

### The evaluation of the IMC generation and cross-sectional status

To confirm the jointing status between high P Ni and solder, these solder mounted test pieces were analyzed by cross-sectional SEM observation.

Figure 7 shows the cross-sectional BSE image which was mounted solder on high P Ni 10 µm deposit by 280 °C, top reflow condition which was shown in Figure 3 (a).

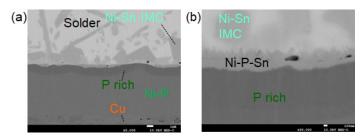


Figure 7: The cross-sectional BSE image of solder mounted on high P Ni 10 µm deposits (a): Low magnification (5k), (b) High magnification (30k).

This was the typical structure of the solder jointing with high P Ni. One can see the Ni-P-Sn reaction layer and P-rich layer generation on the remaining high P Ni layer. The high P Ni thickness was 8 µm and acted as the barrier between Cu and solder. Therefore, Sn couldn't contact Cu and brought excellent bonding strength.

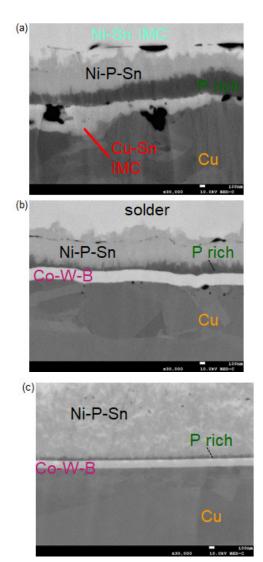
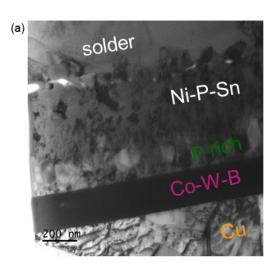


Figure 8: The cross-sectional BSE image of solder mounted on high P Ni 1  $\mu$ m deposit with or without 0.2  $\mu$ m of Co-W-B deposits (30k). (a) Without 0.2  $\mu$ m of Co-W-B deposits (b) With 0.2  $\mu$ m Co-W-B (c) With 0.2  $\mu$ m Co-W-B and soldering under harder reflow.

Figure 8 (a) shows the cross-sectional BSE image of solder mounted with high P Ni 1 μm in jointing by 280 °C, top reflow temperature. This image shows the Cu-Sn IMC generated between the P-rich layer and Cu. Therefore, the bonding strength was poorer than high P Ni 10 μm condition. On the other hand, Figure 8 (b) shows Co-W-B 0.2 μm / high P Ni 1 μm stacked deposits with solder jointing with 280 °C, top reflow temperature. It shows a P-rich layer connected on Co-W-B directly and there was no Cu-Sn IMC generated due to the Co-W-B layer. Moreover, Figure 8 (c) is the cross-sectional image applied harder Figure 3 (b) reflow profile. It showed 0.2 μm Co-W-B deposits withstood as the barrier between Cu and solder under harder reflow such as 300 °C, 10 min. Figure 8 (c) and (b) show differences structurally.

The detail structural and elemental analysis comparison of the solder mounted on Co-W-B / high P Ni stacked deposit jointing with different reflow conditions.

Based on Figure 8 (b) and (c), there were differences structurally by reflow condition. Therefore, it might be that they had a different Ni-Sn IMC generation status.



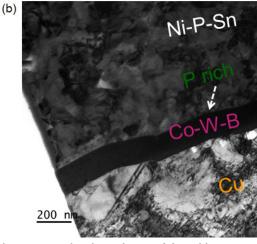


Figure 9: The cross-sectional TEM image of the solder mounted with different reflow profile on Co-W-B 0.2  $\mu$ m / Ni-P 1  $\mu$ m stacked deposit. (a) Solder joint with 280 °C, top reflow. (b) Solder joint with 300 °C, 10 min. reflow.

Figure 9 (b) shows a thinner P-rich layer than Figure 9 (a). Therefore, the IMC generation reaction proceeded between P rich layer and IMC under harder reflow.

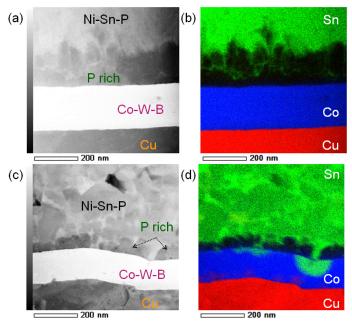


Figure 10: Cross-sectional High-Angle Annular Dark Filed Scanning Transmission Electron Microscope (HAADF -STEM) image and correspondence EDS overlap mapping with Sn, Co and Cu element.
(a) HAADF -STEM image of solder joint with 280 °C, top reflow. (b) EDS map of Figure 10 (a). (c) HAADF-STEM image of solder joint with 300 °C, 10 min. reflow. (d) EDS map of Figure 10 (c)

Figure 10 shows HAADF-STEM image and correspondence EDS map overlapped with Sn, Co and Cu to evaluate the diffusion barrier status between Cu and solder. Figure 10 (b) shows that the solder diffusion was prevented by P- rich layer. On the other hand, Cu diffusion was prevented Co-W-B layer. In Figure 10 (d) the indicated Cu diffusion was still prevented by Co-W-B deposit. Moreover, Sn diffusion proceeded along the grain boundary of the P-rich layer and connected to Co-W-B layer. However, Sn diffusion was prevented inside of Co-W-B layer and didn't connect to Cu even though harder reflow conditions were applied. Consequently, Co-W-B and P-rich layer acted as the double barrier between Cu and solder.

High temperature storage test of Co-W-B / high P Ni stacked deposit after solder joint.

Co-W-B / high P Ni stacked deposit with solder jointing specimen was subjected to the high temperature storage test (HTST) to evaluate the thermal durability. The evaluation sample was plated Co-W-B 0.1 µm / high P Ni 1.0 µm and solder jointing with Sn-Cu-Ni-P type solder by Figure 3 (a) reflow. Table 3 shows temperature and aging time conditions in HTST and the evaluation result of bonding strength and fracture mode by the nut pull test.

Table 3: HTST temperature, aging time condition and the result of bonding strength by nut pull test which evaluated by the average of three tests.

time (h) at 175 °C	Bon	fracture			
0	1176	936	939	997.3	solder
250	903	713	875	830.3	solder
500	988	1074	766	942.7	solder
100	808	758	749	771.7	solder

Based on the above evaluation, Co-W-B / high P Ni stacked deposit kept excellent bonding strength and fracture mode throughout this HTST test. Moreover, Figure 11 shows a cross-sectional BSE image of the specimen which passed each aging time.

Figure 11: The cross-sectional BSE image of the specimen which passed each aging time. (a) 0 h, (b) 250 h (c) 500h (d) 1000 h. Magnification: 30k.

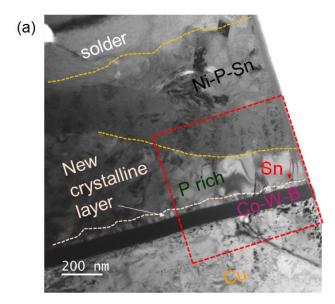
Figure 11 shows there wasn't generation of the Sn-Cu IMC and Co-W-B acted as intermediate barrier between Cu and solder throughout HTST test. However, thinner P-rich area was generated and expanded gradually. It has possibility to proceed the diffusion reaction between P-rich layer and solder.

The detail cross-sectional observation and elemental analysis of thinner P-rich layer area.

In Co-W-B / high P Ni stacked deposit, the P-rich layer generated after solder jointing acted as the barrier for Sn diffusion. On the other hand, the thinner P-rich area expanded gradually in the evaluation of the HTST. This thinner P-rich area was generated by the reaction proceeding between the P-rich layer and the solder. To identify the detail of this reaction proceeding, cross-sectional TEM observation and elemental analysis by EDS was performed using the specimen which was kept for 1000h, at 175 °C in HTST.

Figure 12 shows the cross-sectional TEM image of HTST 175 °C, 1000 h specimen. Figure 12 (a) exhibited thinner P-rich area and (b) showed thicker P-rich area. Co-W-B layer of both areas didn't change the status and Cu diffusion was prevented. On the other hand, the Ni-P-Sn reaction layer was expanding in the thinner P-rich layer area. Moreover, it seemed like the Ni-P-Sn reaction layer was proceeding along with the grain boundary of the P-rich layer and stopped on the thinner new crystalline layer which was generated on the Co-W-B layer.

This thinner new crystalline layer on the Co-W-B layer didn't generate a thicker P-rich layer area. Therefore, it had the possibility to generate new IMC by the reaction proceeding between the P-rich layer and solder.



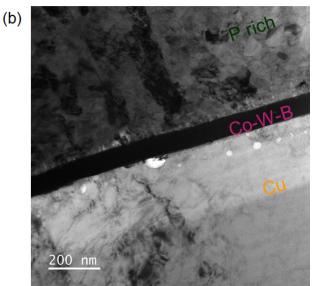


Figure 12: The cross-sectional TEM image of the HTST 1000 h aging of Co-W-B / high P Ni stacked deposit with solder jointing (a) thinner P-rich area (b) thicker P-rich area

To clarify the generation root of a new crystalline layer in the thinner P-rich layer area, EDS analysis was performed. Figure 13 shows the HAADF-STEM image and EDS Co mapping analysis data. Figure 13 (a) is the HAADF-STEM image of the thinner P rich layer area while (b) is its Co mapping data. Figure 13 (a) also shows the Ni-P-Sn reaction layer was proceeding along with the grain boundary of the P-rich layer and stopping on the new crystalline layer alike TEM image. Figure 13 (b) shows that Co was diffused to P-rich layer from Co-W-B in the thinner P-rich area. Therefore, this data indicated the new crystalline layer was including Co and one of its generation root was Co diffusion.

On the other hand, Figure 13 (c) shows the HAADF-STEM image of the thicker P-rich layer area and 13 (d) is its EDS Co mapping data. In Figure 13 (d), Co diffusion was not proceeding so much compared to the thinner P-rich layer area.

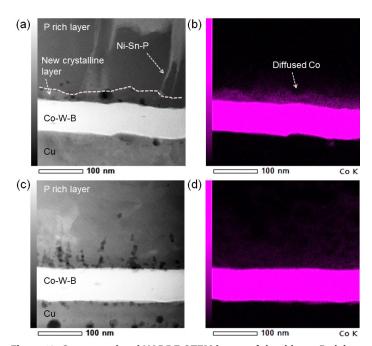


Figure 13: Cross-sectional HADDF-STEM image of the thinner P-rich area or thicker P-rich area and EDS Co map (a) HADDF-STEM image of the thinner P-rich area (b) EDS map of Figure 13 (a) (c) HADDF-STEM image of thicker P-rich area (d) EDS map of Figure 13 (b).

In order to observe and identify the composition of the new crystalline layer on the Co-W-B layer, Bright Filed Scanning Transmission Electron Microscope (BF -STEM) observation and EDS quantitative analysis of this layer were performed in Figure 14.

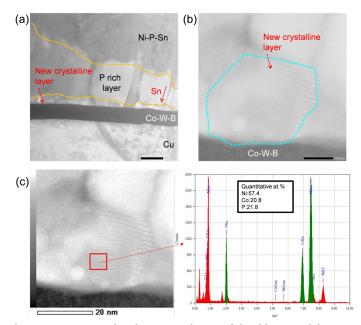


Figure 14: Cross-sectional BF-STEM image of the thinner P-rich area and EDS Quantitative analysis of the new crystalline layer. (a) Low magnification of the BF-STEM image (b) High magnification of the BF-STEM image (c) EDS spectrum and Quantitative analysis.

Figure 14 (a) shows the low magnification image of BF-STEM in the thinner P-rich layer area and (b) shows the high magnification image of the new crystalline layer on Co-W-B layer. Figure 14 (b) shows the lattice fringe and grain boundary in the new crystalline layer. Therefore, this data indicated the layer is a crystalline structure. Figure 14 (c) is the EDS quantitative analysis result of this grain. Based on Figure 14 (c), this new crystalline layer consists of Ni, P, and Co. and the quantitative value was Ni:57.4 at.%, Co: 20.8 at.% and P:21.8 at.% respectively. Overall, this new Ni-Co-P IMC was generated by the Co diffusion to the P-rich layer and it also worked as the barrier for the solder diffusion.

Figure 15 illustrates the estimated mechanism of the Ni-Co-P IMC generation at the thinner P-rich layer area. The reaction between Ni and Sn is generally uneven. Therefore, it is possible to proceed a reaction between Ni and Sn partially. Moreover, the Co diffusion from Co-W-B layer proceeded at the area which Ni and Sn reaction proceeded faster. Consequently, the Ni-Co-P IMC was generated.

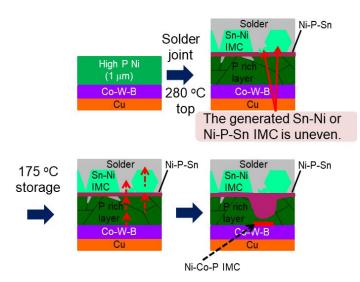


Figure 15: Estimated mechanism of the Ni-Co-P IMC generation at the thinner P rich layer area.

### **CONCLUSIONS**

In this investigation, adding the 0.1 - 0.2 µm of electroless Co-W-B deposits between Cu and high P Ni for the barrier was examined. The following examination was performed: the bonding strength, structural and elemental analysis, and conducting of the HTST.

Based on this investigation, Co-W-B / high P Ni stacked deposits showed excellent bonding strength and Co-W-B prevented the Cu-Sn IMC generation. In structural and elemental analysis, thin high P Ni on the Co-W-B deposits was exchanged to Ni-Sn IMC and P-rich layer after solder joint. Moreover, Co-W-B and the P-rich layer acted as the double barrier between Cu and solder. Furthermore, the new Co-Ni-P IMC was generated at thinner P-rich layer areas. It also acted as the barrier for solder.

Figure 16 shows the investigation summary of Co-W-B / high P Ni stacked deposit for the solder joint. Overall, the Co-W-B deposit acted as the thinner and stronger thermal diffusion barrier for Cu. Moreover, the P-rich layer which was exchanged from high P Ni on Co-W-B deposit acted as the barrier for solder. To use this stacked deposit, high P Ni thickness could be reduced to 1 µm from 10 µm.

In this investigation this new Co-W-B / Ni-P stacked deposits for solder joint was mainly evaluated as the aspect of the thermal durability.

We'll evaluate the extended thermal cycling test as the aspect of durability for the combination of thermal and stress as the next step.

We believe these stacked deposits will provide a benefit for space saving for the packaging and downsizing of electronic devices.

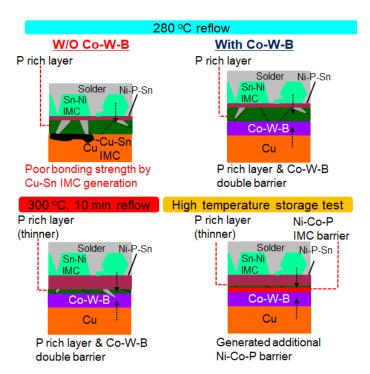


Figure 16: The investigation summary of Co-W-B / high P Ni stacked deposit for the solder joint reliability.

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### **BIOGRAPHIES**



Yoshihito Ii is working for the R&D division in C. Uyemura & Co., Ltd. as an engineer. He received his master's degree at Graduate School of Natural Science and Technology in Okayama University. He developed some electroless plating or pretreatment chemicals and submitted some patents with his co-workers. He recently studied

the diffusion barrier ability of electroless Co-W-B deposits for Cu and gave presentations in some conferences in Japan.

Hiroki Okubo is an engineer at the R&D division of C. Uyemura & Co., Ltd.

Shoichi Fukui is a sales staff at Nagoya branch of C. Uyemura & Co., Ltd.

Tetsuji Ishida is a section director at R&D divison of C. Uyemura & Co., Ltd.

Shoji Iguchi is a section director at the techinical suport group in Nagoya branch of C. Uyemura. & Co., Ltd.

Katsuhisa Tanabe is a manager at R&D divison of C. Uyemura & Co., Ltd.

Shigeo Hashimoto is a senior managing director at C. Uyemura & Co., Ltd.

### **Cleaning Process Simulation by Glass Test Boards**

### Vladimír Sítko

PBT Works s.r.o. Lesní, Czech Republic

### **ABSTRACT**

This article explains the utilization of Glass Test boards for different tasks for the cleaning process building, optimization, and monitoring. We have 12 years of experience building and using Glass Test Boards as a precise tool for comparing material properties, machine settings, and process optimization. Some years ago, we decided to do a joint project with the company, Magnalytix, and build another kind of test board capable of being optical inspected and tested on the surface resistance.

We want to share our experiences and show the advantages of utilizing such glass models for enhancing the quality of the cleaning process and lowering the cost of building the process.

KEY WORDS: Glass test boards, Surface insulation resistance, Cleaning PCBA, Cleaning process optimization, Cleaning process qualification

### INTRODUCTION

Cleaning electronic assemblies has changed dramatically during the past 20 years. The reason is the introduction of new packages, increasing density on the boards, and much stronger requirements on final cleanliness (quality of surface resistance and signal integrity) for a long lifetime. The BTC (Bottom – terminated packages) has brought particular challenges because of its lower gap under the component and much larger gap area than other packages. Besides that, an optical inspection of rest residues is almost impossible.



Figure 1: QFN soldered - after cleaning - checking residues between poles optically is almost impossible.

Finding the optimal parameters for thorough cleaning is not a straightforward process. It requires an optical check of the result and the next test with changed parameters. The fastest way to do it is to tear components from the board. Such operation is mostly connected with damage to the PCB.



Figure 2: Special pliers for tearing components. Each can be used only for a specific type of component.



Figure 3: A trained person can tear the component of the board without board damage

Our experience says that the "hot" method (hot air desoldering) can never show the actual situation under the component. We met situations where a flux from voids "exploded" during desoldering and contaminated the surrounding area. Recognizing that such small flux splashes are not an uncleaned residues is almost impossible.

Pliers cannot tear bottom terminated connections. Heavier techniques must be utilized.

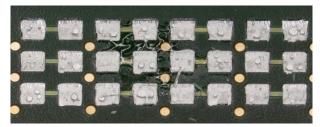


Figure 4: Dismounted joints of daughter board as an LGA connection. Residues and voids are visible.

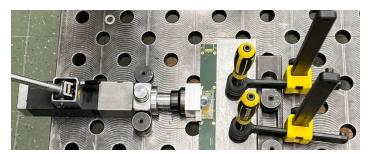


Figure 5: A dedicated hydraulic jig for tearing assembly from Fig. 4

Tearing components is effective from the point of fast process building, however, not from the cost view. Current assemblies might be expensive, as well as some BTC components. Moreover, scraping such material in the time of current delivery problems became less and less popular.

### GLASS TEST BOARDS WITH MATRIX OF PASSIVES

Already in 2008, we developed the prototypes of Glass Test Boards. (GTB) The original purpose was to compare the cleaning efficiency of our products - cleaning machines. Soon, we learned that such a precise tool, reusable, with a long lifetime, can also be used for other tasks in the cleaning process building.

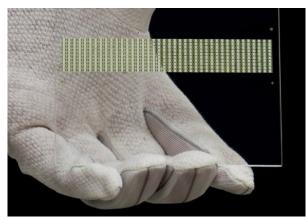
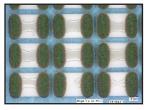


Figure 6: Glass Test board with 400 chips (0805)

Today, we manufacture them for our test purposes, but also customers. They have two passives sizes (0805, 0511) and three gap thicknesses. (35,60 and 70um) An essential difference between them is the different typical times to complete cleaning.



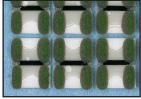


Figure 7: Details of Glass test boards with passives 0805 and 0511 (right side). Half cleaned.

Test preparation is easy. You must deposit three parallel lines of flux from solder paste on the top of the passives matrix. Then reflow it at the same temperature profile as the PCBA. After cooling to room temperature, the Glass Test Board is ready for the test. The test is targeted to cleaning under components. By experiments, it was confirmed that the time to clean the surface and gaps between components is less than 10% of the time needed to clean under chips. Therefore, the method is not sensitive on the surplus of flux which remains on the surface. Always, it is necessary to check optically the completeness of wicking the flux under components (no voids).

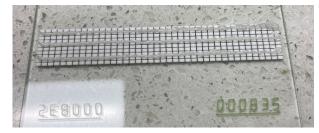


Figure 8: Deposit of solder paste flux before reflow

Test board evaluation of rest residues by the naked eye is not precise enough and always subjective. To increase precision, we have developed a dedicated tool.

### AUTOMATIC OPTICAL TEST SYSTEM FOR GLASS TEST BOARDS



Figure 9: Automatic optical test system VERINAS for evaluation of Glass Test Boards

The test system automatically makes a test protocol. It evaluates all 400 chips in the matrix and gives necessary statistical calculations.

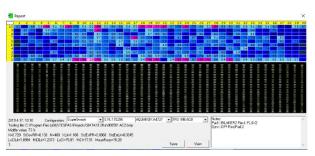


Figure 10: Test report from the Automatic optical system VERINAS

The optical tester measures the ratio of not cleaned area to the area of a complete gap under component. The repeatability of such reading is better than +-5%. Other differences can be caused by changing of reflow parameters. For precise measurement, the reflow conditions and time between reflow and cleaning should be constant.

These Glass Test Boards have multiple use. During the first phase of building a cleaning process (see also IPC CH65B), at least two studies for Cleaning process feasibility can be effectively performed using such a tool.

### MATCHING CLEANING AGENT TO FLUX RESIDUES.

We use a technique of step-by-step (sequential) washing and measuring results after each step. With that approach, we get a record of residue percents under chips during cleaning. We call it a washing curve.

Because our Glass Test Boards are very precise and always the same, we can compare the dynamic solubility of proposed combinations of flux residues and cleaners by keeping all cleaning parameters at the same level.

For one type of cleaner, we can get such data for a virtually unlimited number of solder pastes (in practice, up to 32 in our machines)

Such a study, when performing it on the cleaning machine, can take one shift for one cleaner.

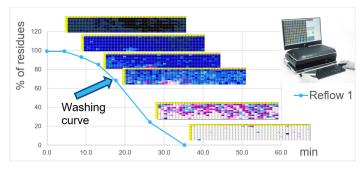


Figure 11: Sequential washing and cleaning curve

To compare the solubility, we introduce a figure, "Cleaning Resistance Value" (CRV) which is proportional to the area under the cleaning curve-

More soluble combinations have the cleaning curve steeper and the area under the cleaning curve smaller. The CRV value is indirectly proportional to the ability of the cleaner to dissolve flux residues.

#### PROCESS CHANGES VALIDATION

Another application of Glass Test Boards is a validation of cleaning process changes. The difference in the cleaning result on the Glass test Board before and after the process change can quickly determine whether the washing (the first step) is better than before the change.

Such a test result can be used as written evidence supported by the figures that the process change did not negatively change the performance.

### WASH PROCESS MONITORING

Periodical cleaning of the Glass test Board can bring actual information of the washing bath condition.

For such measurement, we must choose the flux and type of the Glass Test Board so that the result of rest residues under chips on the Glass Test Board is about 50% after standard wash time. Any deviation from these values is a signal of some change in the activity of the cleaner. Each cleaning cycle gets a certain amount of flux residues, depending on the amount of printed solder paste to the boards. Refreshing by the topped-up cleaner brings a new, active cleaner to the system. The top-up dosing amount is proportional to the drag-over.

When different products run through the machine, the condition of the cleaner can vary in both -side directions.

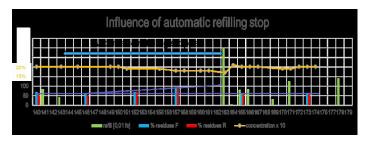


Figure 12: Record from a process monitoring.

During 20 cycles, the concentration dropped by nearly 2% (Yellow line). However, the residues on the Glass Test Board increased by nearly 30%. The blue and red columns are the results of cleaning two GTB. (As a demonstration, we stopped the refilling.) After refilling the cleaner to the initial concentration, the cleaning result got back to the previous values.

### MACHINE CAPABILITY STUDIES

Almost every customer wants to have the machine capability study after installation. Hence customers like to measure all controlled parameters. According to the method for such measurements, at least 50 or 100 values are needed to make results. Measuring bath temperature stability would mean running 50x or 100x from room temperature to the set point. But cooling 100 ltr liquid in the

machine takes about 24 hours. And bath temperature is only one of several parameters which still do not define the result completely. And there is no standard information about the necessary tolerances for each controlled parameter. We have, several times, proposed to measure the machine's capability by cleaning a sequence of Glass Test Boards. At least for the washing section, such an attempt can bring acceptable accuracy in a reasonable time.

Before such measurement, we must determine the cleaning space homogeneity. Many machines have spots in the chamber where the cleaning intensity drops down. Cleaning several Glass Test Boards can quickly give data on such irregularities.



Figure 13: Machine with rotation arms record from washing homogeneity measurement by several Glass Test Boards

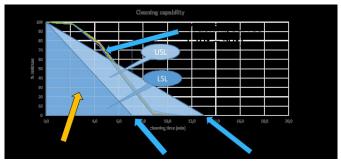


Figure 14: Determination of Cmk from Measuring the Cleaning Resistance Value during several runs of Glass Test Board

For calculating the Cmk, an Upper and Lower acceptable value ( of the washing time) must be defined. The upper time is limited by the chemical compatibility of components, inscriptions, labels, or plating on the boards. Usually, the lower value can be determined during process optimization.

### GLASS TEST BOARDS FOR PROCESS OPTIMIZATION AND PRE-QUALIFICATION

The GTB with chip matrix is suitable for any comparison studies. Its advantage is the possibility of automatic evaluation of cleaning results.

However, some components have specific challenges in cleaning—especially Bottom Terminated Components.

Difficulties in optical evaluation make setting parameters for proper cleaning difficult and expensive.

Therefore, we decided to develop Glass Test Boards, which enable easy checking of residues under packages and, simultaneously, measuring of Surface Resistance.

Some examples of such boards are on the following figures:

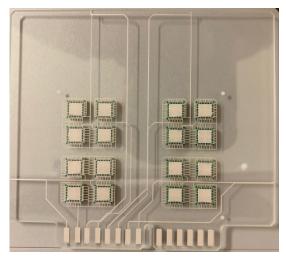


Figure 15: Glass test Board for flux degassing studies with 4x4 QFN44

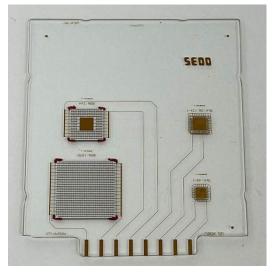


Figure 16: Glass Test Board for cleaning parameters optimization with QFN48, QFN DR124m, BGA244, and BGA 1020.

Such boards can also quickly help to compare the robustness of the No-clean flux system during moisture test. The advantage is a non-destructive analysis of ion migration.



Figure 17: Migration of ions caused by leakage current.



Figure 18: Details of the Dendritic structure of Siver, grown in flux residues during the moisture test 90%rH, 40°C, 169 hrs.

GTB enables observing even tiny changes in the flux residues amount during and after cleaning.





Figure 19: Flux residues (A) before and (B) after the SIR test (169 hrs, 40°C, 90% RH). Mention a reduction of flux residue volume, probably by a continuing degassing process during the test. (in figure B)





Figure 20: Comparing BGA structure (A) before and (B) after cleaning. The gap size is 220um

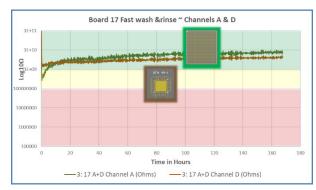
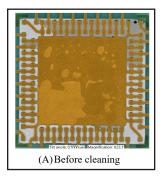
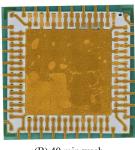


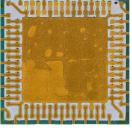
Figure 21: SIR values of QFN and BGA (from Figures 19 and 20)

Sequential cleaning can help to analyse also other factors which can strongly influence cleanability. This is component tilting during soldering. The following pictures show a massive difference in cleaning time in different corners of QFN 124 DR. The cause is a very different gap thickness in those corners. We assume that such tilting can occur by degassing during the soldering process. Too short time for degassing did not allow all gasses to escape before solidification.





(B) 40 min wash



(C) 50min wash

Figure 22: Sequential cleaning shows a slower process in the upper right corner.

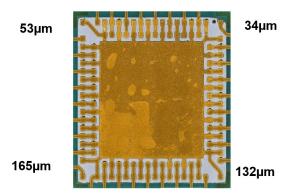


Figure 23: Gap thickness measured by 3D microscope through glass – shows tilting of package during soldering. Flux accumulate un the lowest corner, fully clogged spaces between terminals. Cleaning such components is more challenging.

#### CONCLUSION

Using Glass Test Boards can help optimize processes, both noclean and cleaning.

Glass Test boards with the chip matrix help to speed-up necessary works for new cleaning process building and saves cost for components and PCBs which would have to be scrapped during such tests.

Glass Test Boards with different dummy components can make cleaning process parameter optimization easy and fast. Such optimization can need only one piece of Glass Test Board. Such a board can be cleaned using a sequential cleaning approach. Short washing cycles and repeatedly observing the result determine the necessary time for a wash. Also, the SIR test with the same type of Test board can check the resulting quality.

Glass Test Board can also be used for checking the flux robustness during the surface insulation test. It can discover critical points where the bias potential is highest and induces leakage currents or initiates dendrite growth.

We plan to offer fast service in building Glass Test boards, with some standard configurations of challenging components or customized for unique configurations and types of components.

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- [3] Mike Bixenmann, Dough Pauls, Mark Mc Mean (Professional Development Course: Qualifying and controlling Clean and Noclean processes, APEX 2022
- [4] Mike Bixenmann, Mark Mc Mean, Vladimir Sítko (Climatic Reliability of Electronics, March 2023 CELCORR DTU Denmark) Optical Inspection and SIR measurement under the Component bodies using a SIR Glass Test Vehicle

### **BIOGRAPHY**

Vladimir Sitko is a founder and mentor of PBT Works s.r.o, a recognized manufacturer of electronic assemblies cleaning systems. After finishing his studies at Technical University, he started his career (nearly 50 years ago) as a designer of measuring devices for silicon analysis and machines for chip processing, assembly, and encapsulation.

In the 90s, he gained expertise in soldering, paste printing, and PCBA cleaning. At the same time, he built the first cleaning machines for PCBA cleaning in his company. Cleaning assemblies and tools for microelectronic assembly have become his primary focus until now. More than 30 years of experience gave him much information on increasing the reliability of electronics by cleaning. He participates in several research tasks for cleaning technology. He owns several patents for details of cleaning machines and test tools.

### Comparison of Electromigration in Tin-Bismuth Planar and Bottom Terminated Component Solder Joints

Prabjit Singh<sup>1</sup>, L. Palmer<sup>1</sup>, M. Hamid<sup>1</sup>, R. F. Aspandiar<sup>2</sup>, B. Franco<sup>2</sup>, H. Fu<sup>3</sup>, V. Vasudevan<sup>4</sup>, A. Allen<sup>5</sup>, K. Howell<sup>6</sup>, K. Murayama<sup>7</sup>, H. Zhang<sup>8</sup>, A. Lifton<sup>9</sup>

<sup>1</sup> IBM Corporation, Poughkeepsie, East Fishkill, NY, and Rochester, MN, USA, <sup>2</sup> Intel Corporation, Hillsboro, OR, USA, <sup>3</sup> iNEMI, Shanghai, China, <sup>4</sup> Dell Technologies, Round Rock, TX, USA, <sup>5</sup> HP, Inc., Palo Alto, CA, USA, <sup>6</sup> Nihon Superior Co., Ltd., Osaka, Japan, <sup>7</sup> Shinko Electric Industries Co. LTD., Nagano, Japan, <sup>8</sup> Indium Corporation, Clinton, NY, USA, <sup>9</sup> MacDermid Alpha Electronics Solutions, South Plainfield, NJ, USA

### **ABSTRACT**

Electromigration monitoring of bottom terminated component (BTC) solder joints is limited to electrical resistance measurements of the solder balls. Tracking the microstructural evolution such as bismuth segregation in tin-bismuth solder ball, is typically via metallurgical cross sectioning, a destructive technique. Once cross sectioned, the solder ball is not available for further electromigration current stressing. A novel planar solder geometry has been invented and developed that allows real-time, non-destructive monitoring of solder microstructure, while the progress of electromigration can be concurrently tracked via electrical resistance means. Planar solder joints are easy to fabricate in a typical metallurgical laboratory. If the electromigration behavior of the planar and the BTC solder joints happen to be similar, the planar solder joint approach could greatly aid in the quick development of solder alloys by comparing the rates of electromigration and the metallurgical changes in planar solders of various compositions. In this paper, the electromigration rates and behavior of eutectic Sn-Bi alloy in planar and in BTC solder joints were compared and shown to be similar. This important finding opens the use of planar solder joints for the quick and lowcost development of low-temperature solder alloys.

Key words: Electromigration, tin-bismuth solder, planar solder, bottom-terminated components, solder joints.

### **INTRODUCTION**

When the European Union RoHS edict forced the electronics industry to eliminate the use of lead metal in solders, SAC305 solder became the solder of choice for electronic assemblies [1].

Tin-bismuth solder was considered but rejected because the lead-metal containing finishes on components in the supply chain would have reacted with Sn-Bi solder resulting in a very low melting temperature ternary eutectic [2]. With time as the lead-metal on components in the supply chain got flushed away, the interest in the low melting temperature Sn-Bi eutectic as a solder of choice for electronic assemblies revived for a couple of reasons: One is that at lower soldering temperatures there is less warpage of the assemblies and the second is the energy saving resulting from lower-temperature soldering operations. According to an iNEMI white paper, the deployment of Sn-Bi solder in 1st level packaging is facing two major challenges: high alpha particle emission and electromigration [3].

This paper describes a novel approach to studying electromigration in low-temperature solders such as Sn-Bi eutectic that involves fabrication of a planar solder joint bridging copper traces on a printed-circuit board so that the metallurgical and electromigration phenomena can be directly and non-destructively observed simultaneously with the monitoring of the resistance increase of the solder joint. Planar solder joints of various low-temperature metallurgies can be easily fabricated in a typical metallurgical laboratory and their electromigration behavior quickly and quantitatively studied and compared in a matter of weeks. The validity of the planar solder joint approach in predicting solder electromigration behavior in actual applications such as the bottom terminated component (BTC) solder joints was proven in this paper by showing that the electromigration rates and behavior in planar and in BTC solder joints are very similar.

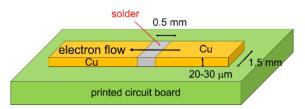
(a)

(b)

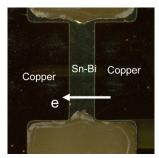
### **EXPERIMENTAL METHODS AND RESULTS**

Planar solder joint fabrication and electromigration testing

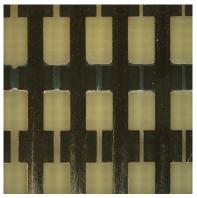
The planar solder joint method for studying electromigration in low-temperature solders has been described in detail in an earlier paper and is described here briefly [4]. Printed circuit boards were fabricated with copper traces with gaps 0.16 to 0.48-mm long and 1.5-mm wide. The gaps were bridged with the solder under test, nominally 30-µm thick, as follows: The gaps were filled with solder paste and covered with 0.1-mm-thick copper foils, followed by reflowing the solder by placing the test assembly in an oven at 180 °C for 12 minutes. The assembly was cooled, the copper foils peeled off and the exposed solder mechanically ground and polished to obtain the finished test specimen shown in Fig. 1.



(a) Schematic of a planar solder joint



(b) Sn-Bi planar solder bridging the gap in a copper trace.



(c) Five Sn-Bi planar solder joints in series. Solder joints had varying lengths to study the effect of solder length on electromigration.

Figure 1: Sn-Bi planar solder joint. The width, length and thickness of the planar solder joints is 1.5 mm, 0.16-0.48 mm and 30-µm, respectively.

The grinding and polishing steps removed all flux residue from the specimens. The resulting test structure consisted of 5 planar solder joints, in series, of varying lengths, to study the effect of solder length on the rate of electromigration. Ten daughter cards, each with 5 planar solder joints, can be plugged into a motherboard as shown in Fig. 2a. The motherboard was wired to allow passage of current through the planar solder joints and the measurement of voltage across the joints using a data logger. With this 4-point resistance measurement approach, resistance can be measured in the micro-Ohm range. An overall view of the test setup is shown in Fig. 2b. Electromigration test runs were conducted at current densities up to 6.6 kA/cm2 in three oven temperatures (60, 80 and 100 °C)

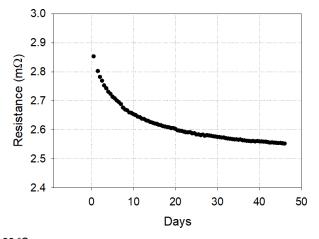




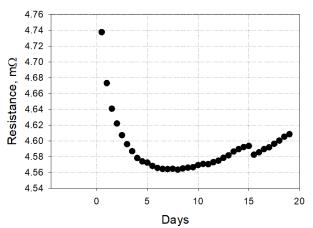
Figure 2: (a) 10 daughter cards plugged in to a motherboard; (b) over all view of test setup.

Accurate measurement of solder joint temperature is critical to the success of an electromigration study. The resistances of the solder joint were measured at a very low current (100-250 mA), low enough to avoid Joule heating, at room temperature and at the temperature of the electromigration test. The coefficient of electrical resistance thus determined was used to calculate the temperature of the solder joints at the start and the end of each electromigration test run.

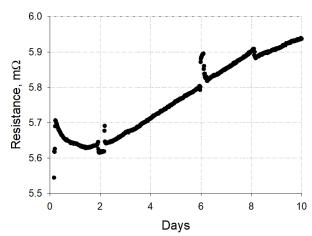
The rates of electromigration in the planar solder joints were measured two ways: (1) rate of change of solder joint electrical resistance as shown in Figures 3 and 4 and (2) rate of increase of the length of the segregated bismuth at the anode as shown in Figures 5 and 6.





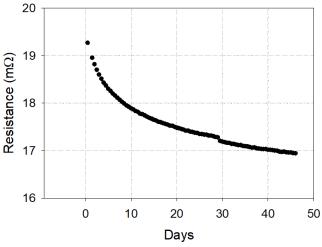


(b) 80 °C oven

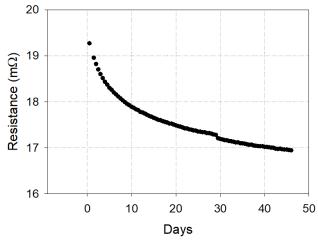


(c) 100 °C oven

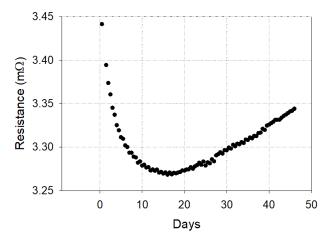
Figure 3: Effect of oven temperature on the temporal resistance behavior of planar solder joints at 1 Amp current (2.2 A/cm²).



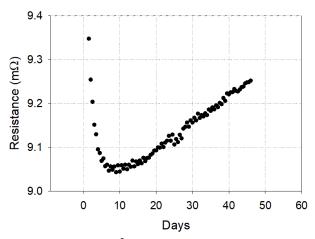
(a) 0.1 Amp current (0.2 A/cm<sup>2</sup>).



(b) 1 Amp current (2.2 A/cm<sup>2</sup>).



(c) 2 Amp current (4.4 A/cm<sup>2</sup>).



(d) 3 Amp current (6.6 A/cm<sup>2</sup>).

Figure 4: Effect of magnitude of current on the temporal resistance behavior of planar solder joints in 60 °C oven at (a) 0.1 Amp current (0.2 A/cm²); (b) 1 Amp current (2.2 A/cm²); (c) 2 Amp current (4.4 A/cm²) and (d) 3 Amp current (6.6 A/cm²).

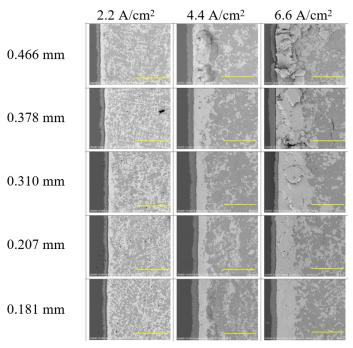


Figure 5: Scanning electron micrographs of eutectic Sn-Bi planar solder joint in 100°C oven. The yellow scale bar is 50-µm long. Electron current flowed from right to left. The lighter phase is Bi rich and the darker phase is Sn rich. The left column lists the joint gaps.

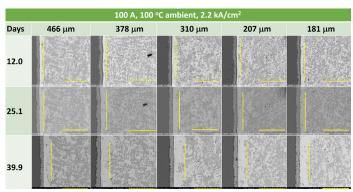
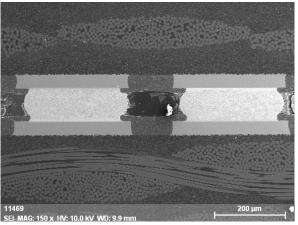


Figure 6: Scanning electron micrographs of eutectic Sn-Bi planar solder joint in 100 °C oven showing the extent of segregation as a function of electromigration time from 12 to 40 days and the solder joint length varying from 0.181 to 0.466 mm. Electron current flowed from right to left. The lighter phase is Bi rich and the darker phase is Sn rich. The left column lists the joint gaps.

### Bottom-terminated component solder joint fabrication and electromigration test

The bottom-terminated component (BTC) solder joints were fabricated to bridge two stacked printed circuit cards. Figure 7 shows a 5x5 mm printed circuit card, representing a component, on the top of a daughter card with an edge card connector that plugs into a motherboard from where wires lead to power supplies and a data logger. The 38 solder joints between the two cards form a square so that the 5x5-mm card floats parallel to the daughter card during the solder reflow step. Only 4 of these solder joints come into play during the electromigration step as explained in Fig. 7. The tops of these 4 solder joints are electrically shorted on the 5x5-mm card side. The circuitry on the daughter card allows the electromigration current to only flow through the solder joints 2 and 3. The voltage across solder joint 2 is measured on the daughter card side between pads 1 and 2; and the voltage across joint 3 is measured on the daughter card side between pads 3 and 4. No current flows though solder joints 1 and 4. Thus, the resistances of the solder joints 2 and 3 are measured using the 4-point approach.



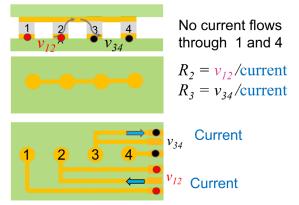
(a) Solder joints (0.60x0.25 mm²) between a component on top and PCB on the bottom.



(b) Top view of a BTC test specimen.



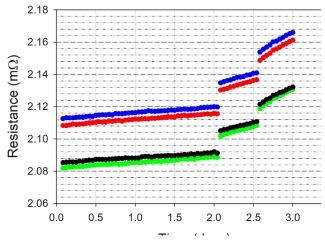
(c) View of test printed circuit board with the top component not shown.



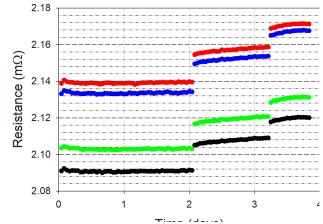
(d) Explanation of the 4-point resistance measurement of solder joints 2 and 3.

Figure 7: Bottom terminated test setup for studying solder joint electromigration.

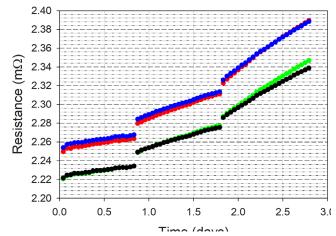
The rates of electromigration in the BTC joints were tracked electrically as changes in the electrical resistance of the joints as shown in Figures 8 and 9. Two daughter cards, each with 2 solder joints, were employed in the test under 4 oven temperatures starting with 100 °C, followed by 80 °C, 120 °C and lastly at 60 °C. Figure 10 shows an example of BTC solder joint cross sectioned after some electromigration stressing. The migration of the Bi towards the anode and its depletion on the cathode side is evident.



(a) 100 °C oven.

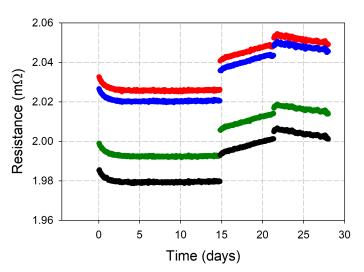


(b) 80 °C oven.

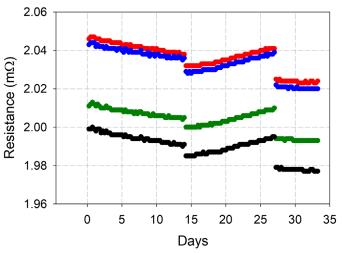


(c) 120 °C oven

Figure 8: Bottom terminated component (BTC) solder joint resistance versus time as a function of oven temperature and current. Data for 2 daughter cards, with two solder joints on each card, are shown. The curves are over three-time periods; the first at 2 A, the second at 4.2 A and the third at 6.2 A current. The sequence of testing started with testing in 100 °C oven followed by 80 °C, 120 °C and 60 °C. The 60 °C test run results are shown in Fig. 9.



### (a) Second test run in 60 °C oven



### (b) Second test run in 60 °C oven

Figure 9: This figure is a continuation of Fig. 8. Above test runs in  $60\,^{\circ}$ C oven were after those shown in Fig. 8. The curves are over three-time periods; the first at 4.2 A, the second at 6.2 A and the third at 2 A current

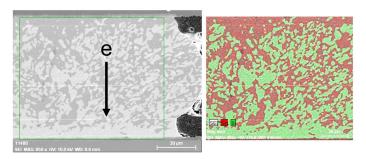


Figure 10: Scanning electron micrograph of a BTC solder joint cross section and an elemental map of the cross section. The green region is Bi-rich phase and the orange region is Sn-rich matrix.

Let us address the question of how best to summarize the electromigration results so that they are useful in predicting the electromigration life of a solder joint: Let us start with Nernst-Einstein equation [5] relating the bismuth atomic drift velocity to bismuth material properties (diffusion coefficient D, effective valence  $Z^*$  and resistivity  $\rho$ ) and to the electric current density j and temperature T.

Rearranging terms, we get

$$v = \frac{DF}{kT} = \frac{DZ^* eE}{kT} = \frac{DZ^* e\rho j}{kT}$$

$$\frac{vT}{i} = \frac{DZ^*e\rho}{k} = \frac{D_0Z^*e\rho}{k}e^{-\frac{Q}{kT}}$$

where Q is the diffusion activation energy. With the reasonable assumption that the bismuth atomic drift velocity v is proportional to the rate of change of resistance of the solder joint, we can say that , leading us to the final equation we can use to summarize the entire electromigration data in the form of an Arrhenius plot,

$$\frac{\left(\Delta R/days\right)T}{j} = Ae^{-\frac{Q}{kT}}$$

where A is just a constant of proportionality [6].

The results of the planar and the BTC solder joints are summarized in Fig. 11. The Arrhenius plot shows the effect of current density and solder temperature on the rate of electromigration.

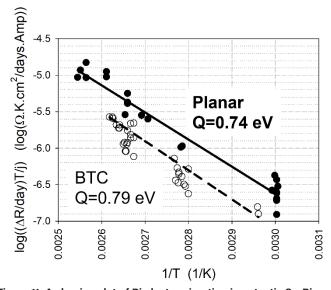


Figure 11: Arrhenius plot of Bi electromigration in eutectic Sn-Bi solder using the planar and the BTC approach.

### **DISCUSSION**

Before we discuss the electromigration results, let us explore the Sn-Bi phase diagram and the kinetics of the Sn-rich phase achieving

thermodynamic equilibrium, that is, achieving the composition predicted by the solvus line on the Sn-rich side of the binary phase diagram shown in Fig 12. The Sn-rich phase has ~ 21 wt. % Bi dissolved in it at 138 °C, a little below the eutectic temperature of 138.5 °C. As the temperature decreases below the eutectic, the equilibrium concentration of Bi in the Sn-rich phase follows the solvus line, decreasing from ~ 21 wt % at 138 °C to ~ 2 wt. % at room temperature. However, the as-cast, rapidly cooled, nonequilibrium structure of Sn-Bi eutectic would retain most of the ~21 wt % Bi in the Sn-rich phase at room temperature. With time, the thermodynamic driving force would lower the Bi concentration in the Sn- rich phase, via the Bi atoms diffusing to the Bi-rich particles dispersed in the Sn-rich phase matrix and to some extent by Bi particles precipitating in the Sn-rich phase. The rate of this drive to equilibrium would be slower at lower temperatures. The time required for the Sn-rich phase to achieve equilibrium composition as per the solvus line would be approximately equal to  $\tau = l^2/\pi^2 D$ , where l is the half the mean size of the Sn-rich phase regions between the Bi-rich particles and D is the diffusion coefficient of Bi in polycrystalline Sn [7]. In the section on homogenization, Reed-Hill describes the relaxation time  $\tau$  as the time required to make a function that depends exponentially on time to decrease in value by a factor of 1/e.

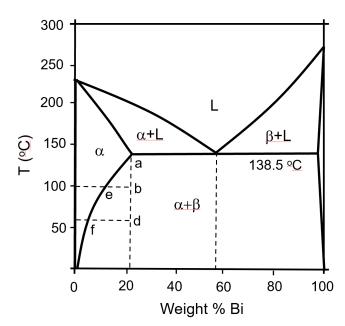


Figure 12: Sn-Bi phase diagram

Electromigration in Sn-Bi solder involves bismuth atoms drifting faster than the tin atoms, resulting in bismuth segregation on the anode side of the solder and loss of bismuth on the cathode side. Given enough time, a Bi-rich phase develops a continuous layer on the anode side while the cathode side gets depleted of the Bi-rich phase. Meanwhile, as the Bi atoms are migrating towards the anode side, the as-cast eutectic non-equilibrium structure evolves by the excess bismuth in the Sn-rich phase diffusing to the Bi-rich particles

and to some extent precipitating out in the Sn-rich phase. The resulting purer state of the Sn-rich phase makes it electrically more conductive. Therefore, from the point of view of the solder joint resistance change, two phenomena are occurring: The Sn-rich phase is becoming purer and therefore more conductive, contributing towards the decreasing of the resistance of the solder joint; and the electro migrating Bi atoms are segregating towards the anode forming a uniform Bi layer and thus contributing towards increasing the resistance of the solder joint. The duration of this initial stage is the time it takes for the Sn-rich phase to homogenize and achieve the composition predicted by the solvus line which is approximately equal to  $\tau = l^2/\pi^2 D$ . This initial stage can be cut short by the Bi atoms segregating on the anode side to form a continuous layer. Once a continuous Bi layer forms, the solder joint can be described as a low resistance Sn-rich phase matrix in series with a high resistance Bi layer. The joint resistance is now dominated by the Bi layer and increases with time as the Bi layer thickens.

The effect of temperature on the duration of the period of decreasing resistance in the early stages of electromigration in planar solders is shown at three different oven temperatures at 1 A electric current in Fig. 3. As the oven temperature increases, the initial period of decreasing resistance shortens. This effect can be explained based on the dependance of the relaxation time  $\tau$  on temperature as listed in Table 1. The magnitude of  $\tau$  at various temperatures in Table 1 is similar to that of Fig. 3. So in summary, the reason for the decreasing solder joint resistance during the early stage of electromigration is the reduction of the Bi content of the Sn-rich phase matrix through with most of the electric current flows.

Table 1: Time for the Sn-rich phase to achieve equilibrium composition as per the solvus line. The diffusion D values are from reference 8.

Temperature, °C	D (cm <sup>2</sup> /s)	$\tau = l^2/\pi^2 D$ (days)	
60	10 <sup>-12.6</sup>	42	
80	10 <sup>-11.6</sup>	4	
100	10 <sup>-10.2</sup>	1.6	

The effect of electric current on the temporal behavior of planar solders in 60 °C oven is shown in Fig 4. At higher currents, the initial period of decreasing resistance is shorter. The effect of the magnitude of current can be explained based on research on electro-dissolution of the Bi-rich phase in Sn5Bi alloy [9]. In this work, it was shown that high currents can result in the dissolution of the Bi from the Bi-rich phase into the Sn-rich phase matrix thus increasing the electrical resistance of the Sn-rich phase matrix through which most of the current flows.

The BTC electromigration tests were conducted on only 4 solder joints. These solder joints were subjected to 2, 4.2 and 6.2 A currents in sequence with oven temperature first at 100 °C, then at 80 °C followed by 120 and 60 °C. The effects of oven temperature and current on the resistance behavior BTC solder joints are shown

in Fig. 8 and 9. The electromigration test runs at 80 °C and above show no period of decreasing resistance. Following these relatively high oven temperature runs, the 4 solder joints were tested at 60 °C oven temperature. Following the test run at 120 °C, the run at 60 °C and 2 A current showed a long period of decreasing solder joint resistance similar to that observed in planar solder joints. The explanation for this period of decreasing resistance is the same as that for the planar solder joints. However, a new phenomenon was observed in these 4 BTC joints at 6.2 A current in 60 °C oven: It was repeatedly observed that the resistance decreased with time under only this specific condition of 6.2 A current in 60 °C oven. More work is need to explain this anomalous but very interesting behavior.

The results of this work summed up in the Arrhenius plots of Fig. 11 prove that the electromigration behavior of planar and BTC solder joints are similar within the limits of the experimental error. The validation of planar solder joints as a reliable vehicle to rank solder alloys from an electromigration point of view is a boon to the rapid development of solder alloy metallurgies with low propensity for electromigration.

### CONCLUSION

The study concluded that the planar and the bottom terminated component (BTC) solder joints have very similar electromigration behavior. They both show an initial period of decreasing electrical resistance in the early stages of the test under low temperature and low electric current density conditions. At high temperatures and high current densities this initial period of decreasing electrical resistance shortens. The Arrhenius plots that conveniently sum up the effect of temperature and current density on electromigration are also very similar for the planar and the BTC solder joints.

Planar solder joints are easy to fabricate. They allow the monitoring of electromigration and microstructure changes simultaneously with electrical resistance changes. BTC solder joints are much more complicated to fabricate. In addition, the electromigration behavior of bottom terminated component solder joints can only be tracked by their electrical resistance. The conclusion that the electromigration behavior of planar and BTC solder joints is similar is very beneficial: It allows the use of the easier to fabricate planar solder joints to study the electromigration behavior of various solder metallurgies. The development of solder metallurgies can thus be greatly shorted and can be conducted at much lower cost.

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#### **BIOGRAPHIES**

Prabjit Singh is a Senior Technical Staff Member in IBM Poughkeepsie, with 45 years of experience in the metallurgical engineering aspects of mainframe computer power, packaging, cooling and reliability. For many years he taught a graduate course on Power Electronics at The State University of New York at New

Paltz. He authored the ASHRAE book on data center gaseous and particulate contamination. He has 88 issued patents and is an IBM Master Inventor. He is a Distinguished Alumnus of the Indian Institute of Technology and an iNEMI Fellow.

Prabjit received a B.Tech. degree in Metallurgical Engineering from the Indian Institute of Technology followed by a M.S. and a Ph.D. in Metallurgy from the Stevens Institute of Technology, Hoboken, New Jersey. Later. he received two master's degrees, one. in microelectronics and the other in electrical engineering.





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